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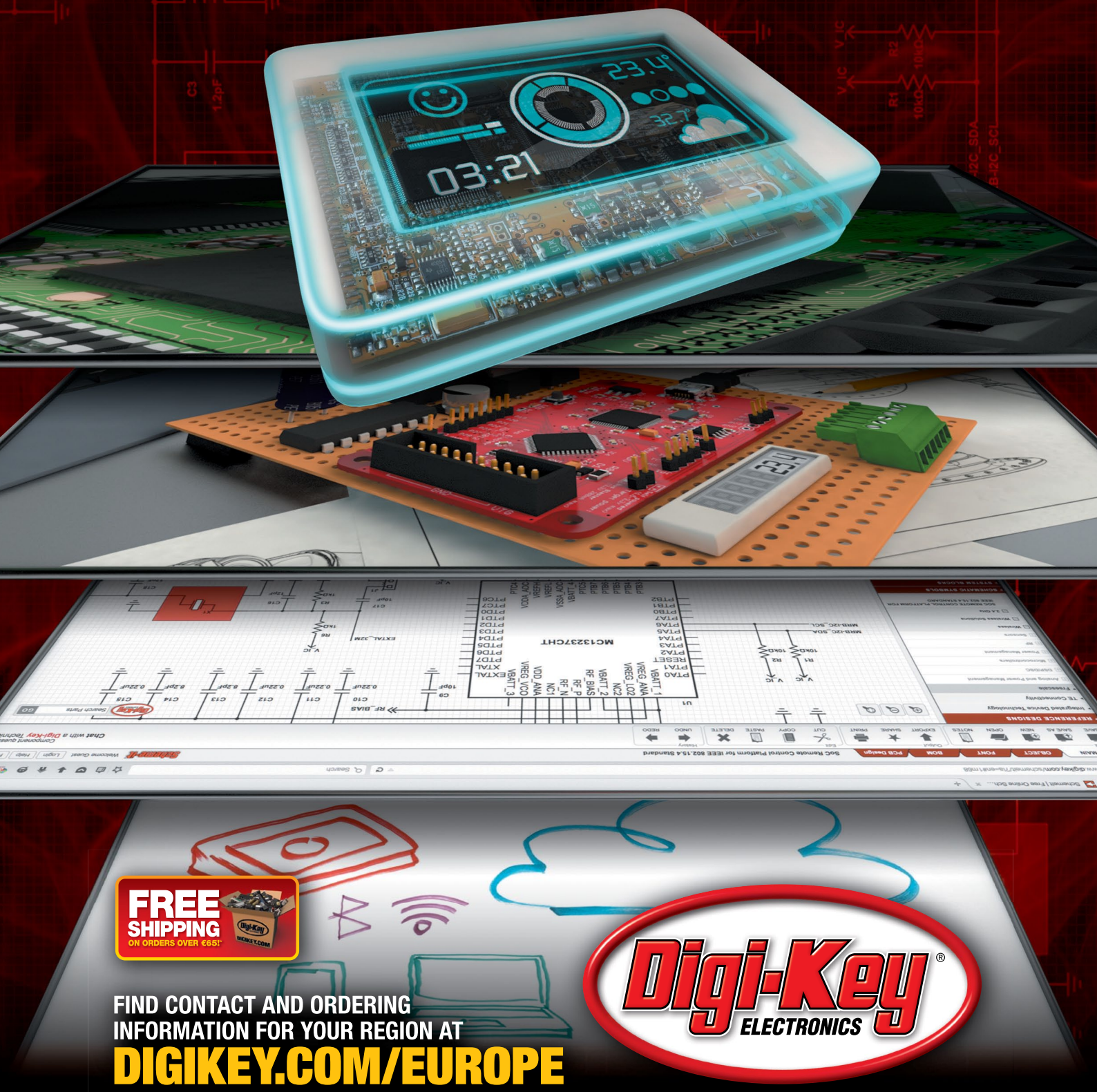

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CONTENTS

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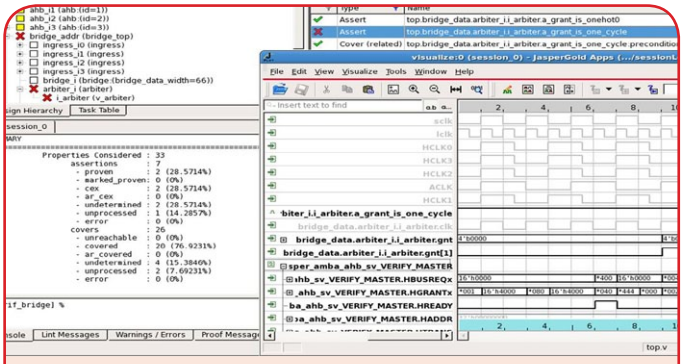

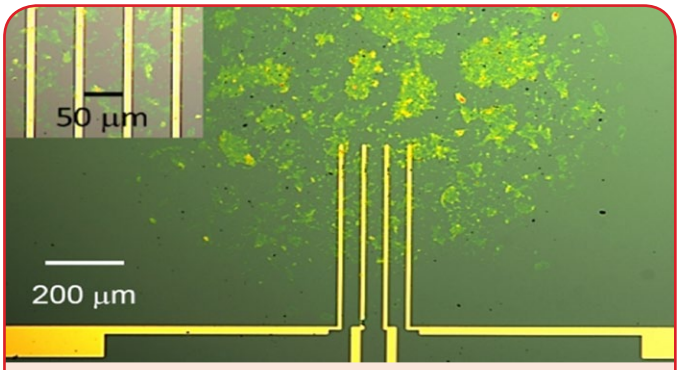

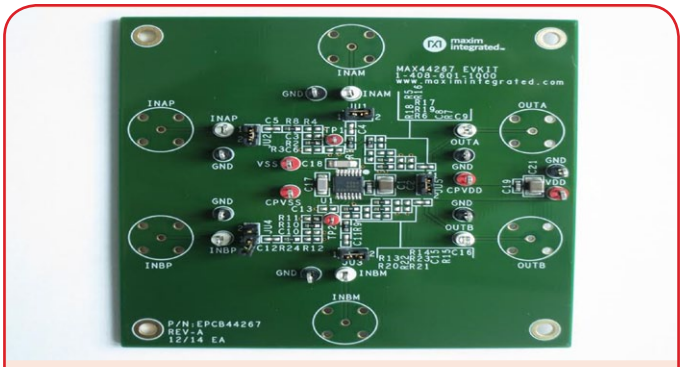

24/7 drone surveillance as a cloud service

By Julien Happich

Last december were taking place in Paris the finals of EIT Digital's Cyber-Physical Systems Idea Challenge. Held at the newly refurbished Pierre & Marie Curie University, the event's highlight was the finalists' pitches, revealing interesting companies in the making.

Drones were on the agenda with French startup UAVIA disclosing a compelling drone-based monitoring service for industrial sites, breaking free of today's radio control limitations while supporting 24/7 drone surveillance as a cloud service.

The six month old startup buys drones and electronic parts (including sensors) to build custom GSM-enabled drones that can be remotely controlled through the GSM network using cloud-based applications. But this is only half of the equation, UAVIA offers to setup up a number of recharging drone stations across the industrial site to be monitored, so that the drones stay on site. The operators do not need to be within radio control range, that is, they could sit in any office instead of having to travel to remote industrial sites.

Co-founder and CEO Clément Christomanos boasted that they had proven the concept flying a drone in Paris while being in San Francisco, using an internet-connected laptop.

When a drone is low on batteries, it returns to the nearest charging station where it can land safely and self-centre itself mechanically within the charging station (thanks to a patented funnel-like connector setup).

The cloud operation comes with various aerial surveillance and inspection tools, making it possible for customers to collect and analyze aerial data from HD video in real time, from their desk. On the company's roadmap is more embedded vision capabilities for automated inspection routines which could see the drones operate without supervision, only sending alerts when detecting intrusions or set visual or topographical changes within the surveyed area.

The captured data is encrypted and uploaded to the company's cloud servers via the connected charging stations, and for remote locations that would not already have 3G/4G LTE coverage, UAVIA has struck a strategic partnership with Air-Lynx, a provider of private LTE networks, to offer a complete package.

"Radio control latency is only 100ms", explained Christomanos, "instead of the typical 6 to 7 seconds latency you would get for satellite-controlled military drones".

"The beauty of this, is that you could have any expert intervene to assess a live video feed. A qualified operator could even hand-over the camera control while maintaining the drone in a hovering mode", commented Christomanos, "so you could share the video stream for closer inspection by third parties. This is typically not possible with today's closed loop systems where only the operator gets the video feed" concluded the CEO.

UAVIA delivers the drone-surveillance as a cloud service, with a setup fee depending on the number of drones and charging stations followed by a 10k euros monthly fee per drone for a hassle-free 24/7 support, maintenance and access to the data analytics tools (this include operator training)

The startup has already secured several contracts with industrial partners which it couldn't name yet. It hopes to beat many of the alternative drone-based site surveillance and inspection companies on a market evaluated to circa 1.3 billion Euros for Europe alone. The startup came second during the final, receiving 25,000 € in prize as well as a free access to EIT Digital's pan-European innovation network (with more than 130 partners), and international growth support through the EIT Digital's Business Development Accelerator. It will also benefit from the network's Co-Location Centres as a base for its internationalization strategy (with co-working space at their discretion).

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BrainChip provides details of neural network architecture

By Peter Clarke

Peter van der Made, CTO and interim CEO of BrainChip Inc. (Aliso Viejo, Calif.) has provided more details of his company's spiking neural network architecture, SNAP64. The company's technology is known as SNAP standing for Spiking Neuron Adaptive Processor.

One of the main differences between BrainChip's implementations and some other neuromorphic processors implemented in both hardware and software is that Peter van der Made has attempted a closer modelling of biological neural networks; including the spike train method of data transfer and modelling of multiple modulations of signals at the synaptic connection.

"The number of neurons and synapses is configurable in the RTL. We could put as many as 10,000 neurons and 5 million synapses on a single die. These are neurons that behave like biological neurons with multiple spiking modes and dynamic, temporal integrating synapses," said Van der Made in email communication with *EE Times Europe*.

Peter van der Made, CTO and interim CEO of BrainChip Inc.

He added: "The neurons and synapses are not multiplexed – unlike other designs like IBM's TrueNorth which are multiplexed 256x and do not learn."

"The advantage of not multiplexing is that they are thousands of times faster, that all memory can be distributed, which simplifies the learning method. The learning method we use is STDP – Spike Time Dependent Plasticity, which constantly accesses memory," said Van der Made.

The use of distributed memory located at the synapses means that SNAP64 is capable of updating neurons at a rate of millions per second and this has been taken up to 4Mupdates/s in an FPGA implementation, Van der Made said.

The circuit implementation of SNAP64 is all-digital although the spikes are spatially and temporally distributed and asynchronous. The SNAP64 RTL has been implanted on a FPGA board from Dini Group La Jolla Inc. (La Jolla, Calif.) with multiple 20 million gate Xilinx FPGAs.

"The SNAP64 architecture is designed to access 65536 (64k) neurons within the same chip, and chips can be stacked to a total of 2^48 = 256B neurons. SNAP64 is fully configurable; the neurotransmitter type and level, neuro-modulators, synaptic connections, and neuron type can be configured through a microprocessor interface. Alternatively, these parameters can be set in the RTL for a dedicated design," wrote van der Made.

Van der Made also provided information on the resolution of potentials in the various parts of the neural network: "Synapses are at this time 18 bits wide, but there can be thousands of synapses contributing to the membrane potential of the neuron. The integrator in the dendrites is 22 bits wide, and the soma integrator is 24 bits wide. These component widths are easily configurable in the RTL if we need more or less resolution."

Finally he pointed out that it is necessary to communicate with the world external to the SNAP64.

"To communicate with a computer we need labelled data. For that purpose we have incorporated sensory neurons that take values in and output spikes, and motor neurons that take spikes in and output values."

Van der Made has written a book, published in 2012, containing a general introduction to neural network technology called Higher Intelligence. It is available from Amazon in print and electronic versions (www.higherintelligencebook.com).

Applications for the SNAP64 technology include speech- and speaker-recognition, visual and image recognition, robotics, drones and automotive systems. BrainChip says on its website that it is currently focused on a set of applications that have been prioritized after consultation with potential partners in California. These applications are in the areas of smartphones, Internet of Things and robotics.

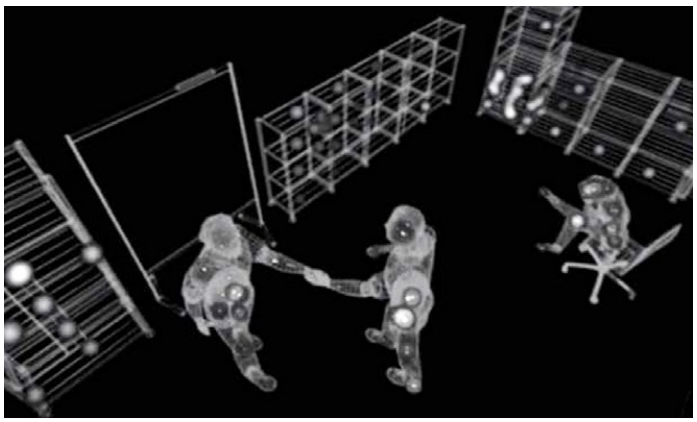
Bat-inspired ultrasound 3D mapping could equip drones

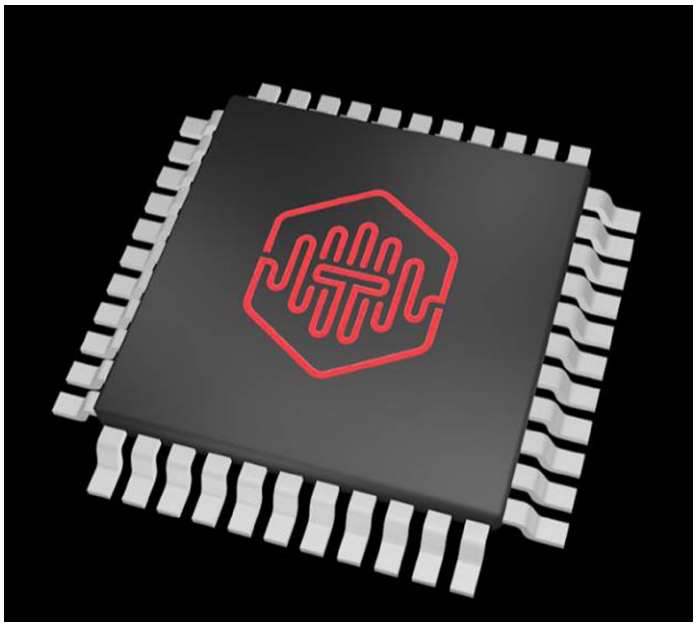
By Julien Happich

German startup Toposens has developed a lightweight and low-cost 3D sensor system that performs ultrasound echolocation and turns the acquired signal into tangible 3D scenery mapping, for either humans or robots to interpret.

Pitching as one of the eight finalist startups at EIT Digital's Cyber-Physical Systems Idea Challenge, co-Founder and Managing Director Tobias Bahnemann attributed the tiny system a sensing range of 4 to 5 meters with a resolution down to 0.5cm, though he is confident he could reach a detection resolution down to 1mm by pushing signal processing further.

Bahnemann had brought with him a compact prototype packaged in a printed plastic enclosure only about 40x40x5mm in size. Weighing a mere 20 grams, the whole sensor solution





combines a piezo-electric ultrasound emitter and three discrete piezo-electric transceivers. Signal patterns are emitted at 40kHz and the time-of-flight of all the echoes are picked up distinctively by the three transceivers, at a nanosecond-level time resolution.

"All of the hardware comes of-the-shelve, told us Bahnemann, "but the key IP resides in the clever algorithms we developed to perform a sort of reverse triangulation and translate the received signals into distance and shape attributes". "These algorithms involve a lot of complicated Maths, yet with a simple hardware setup, we are able to acquire about 50,000 points per second", he commented, attributing the algorithms to co-founder and business partner Alexander Rudoy.

The algorithms took just over three years to develop before the two entrepreneurs were able to showcase a proof-of-concept back in March 2015.

Bahnemann sees uses cases not only in robotics to navigate through complex 3D environments, but also for motion detection and gesture control detection. Because the sensor module requires no optical components and is lightweight, it could substitute expensive and bulky laser and camera-based systems while drawing a mere 0.2W for operation and at a fraction of these systems' price.

Another added benefit of ultrasounds is that it preserves privacy, the results are grey-scale and only reveal depth. Compared to cameras, the sensors are unobtrusive, yet they could be used in shopping malls for customer behaviour analysis as well as for automotive anti-collision systems.

Toposens aims to provide a software development kit during the first half of 2016 for potential application developers to integrate the 3D sensor technology into their products, with various interfaces and software applications at hand.

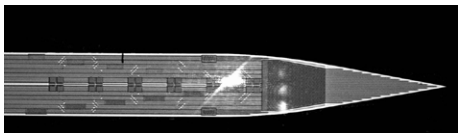
The company was only founded three weeks ago and is actively seeking investors to fund the industrialisation of its sensor. Further on its roadmap, the startup is also aiming to develop a long range 3D radar, capable of providing real time 3D images of the surrounding areas at distances up to about 150-300m for autonomous driving applications.

CMOS-based neural probes tackle single neurons

By Julien Happich

At last IEEE International Electron Devices Meeting 2015, nanoelectronics research center imec, KU Leuven, and Neuro-Electronics Research Flanders (NERF, set up by VIB/KU Leuven and imec) presented a set of silicon neural probes that combine 12 monolithically integrated optrodes using a CMOS compatible process.

The probes enable the optical stimulation and electronic detection of individual neurons, based on optogenetics techniques. They pave the way to a greater understanding of the brain and towards novel treatments for brain disorders such as Alzheimer's, schizophrenia, autism, and epilepsy.



Probe tip with activated light output

Currently available devices for recording neural activity to study the functioning of the brain typically have a limited number of electrical channels. Additionally, the brain is composed of many genetically and functionally distinct neuron types, and conventional probes cannot disambiguate recorded electrical signals with respect to their source.

The researchers' novel neural probes tackle these challenges, opening a new route towards greater understanding of the brain, while enabling novel treatment options for brain disorders.

The new probes combine electronics and photonics to perform extremely sensitive measurements. The fully integrated implantable neural microsystems have advanced capabilities to detect, process and interpret neural data at a cellular scale. The systems feature a very high density of electrodes and nanophotonic circuits (optrodes). Such optrodes are used to optically stimulate single neurons using optogenetics, a technology in which neurons are genetically modified to make them light-sensitive and thus susceptible to stimulation through light pulses.

This research is supported by the Agency for Innovation by Science and Technology in Flanders (IWT) through the Opto-Brain project.

Free core, some assembly required

By Rick Merritt

It's early days for RISC-V - a free, open-source core seen as the Linux of microprocessors. On its long to-do list, engineers still need to define basic pieces of the instruction set architecture including its memory model, how it will speak to the external world of I/Os and how to debug it.

Many of the about 150 developers who signed up for the third RISC-V workshop volunteered to start a handful of working groups to address the most pressing issues in fundamental areas including security, virtualization and compliance.

Proponents said the effort has taken the vanguard of the open source hardware movement, attracting leaders of earlier OpenCore and OpenRISC efforts.

The LowRISC project at the University of Cambridge is attracting interest as the likely first source of real development hardware. The team which includes members of the Raspberry Pi project hopes to have first silicon this year and plans to make low cost development boards available in 2017.

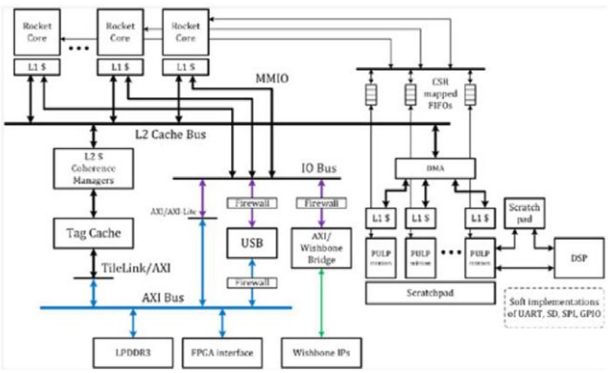
The first of several planned LowRISC chips will tape out before the end of the year, a 3mm2 28nm part that fits in BGA package. It will use four cores running at less than a GHz with 512 Kbytes L2 cache and a 32-bit LPDDR3 memory controller. The group ultimately aims to deliver a low-cost board made completely with open source digital logic.

Until LowRISC is available, developers will work with a handful of emerging system simulators and soft cores mainly implemented in FPGAs. One engineer said he is 80% done with a QEMU emulator for RISC-V that could be completed in two weeks.

Such tools will be key for the biggest job ahead, creating a software ecosystem for RISC-V. Ports of a handful of Linux variants including FreeBSD are well underway as are other low-level components, but ports of more widely used RTOSes and Android are more than a year away.

Ultimately, the effort must attract the broader world of applications developers if it is to become commercially significant.

"We need more developers and more documents and specifications to reduce their startup costs," Arun Thomas, an R&D engineer at BAE Systems told attendees.



So far, developers from seven universities and companies including BAE, Bluespec, Google, LG Electronics and Vectorblox have made 48 software contributions to RISC-V on GitHub. Thomas rattled off a laundry list of needs ranging from specs for direct-memory access, an I/O memory management unit, performance counters, an applications binary interface, bootloaders, hypervisor and security extensions as well as the kind of detailed programming guides ARM provides its users.

"There's a fair amount of work ahead just on the spec side," Thomas said.

A basic port of FreeBSD was created from scratch with 25,000 lines of fresh code written in the last six months, reported Ruslan Bukin, a researcher at the University of Cambridge. This year the group aims to add support for multicore architectures, floating point units, Ethernet drivers and expanded virtual addresses.

Small companies seek ARM alternative

The good news for RISC-V is it has attracted a core of seasoned engineers enthusiastic about the project's potential. For example, Jon Masters, chief ARM architect for Red Hat, took a vacation day to attend the workshop and volunteered to lead a key task group defining a platform specification.

Masters said hopes to write a book about porting Linux to the first commercial open source core. Others said the event marked a historic moment in what will likely be a ten-year process to establish a free microprocessor, disrupting the semiconductor industry in ways Linux upended the software world.

"Everyone wants a free Linux core," said Andreas Olofsson, chief executive of semiconductor startup Adapteva, who joined the fledgling platform working group.

In today's cost-squeezed environment, any company would adopt a free control core then try to create differentiation in software or other hardware blocks, said Olofsson who sported a beard that is a sign he is well along in working on his next-generation Epiphany processor.

Engineers from small companies say they cannot afford the several million dollars required to license an ARM core, several weeks to negotiate the license and a man-year of engineering to integrate it into an SoC. Using roughly similar engineering resources, they can modify RISC-V to suit their needs, something not allowed under a standard ARM license, Olafsson said noting Adapteva is already contributing to and drawing from open-source hardware efforts.

Bigger companies are already kicking the tires. For example, the chief technologist of Chelsio and a member of Microsoft's silicon group attended the event.

"I could see how pretty quickly a RISC-V core could be useful for something simple like a security processor that doesn't need to run a full operating system," said Eric Mejdrich, a principal hardware architect from the group developing chips inside the Xbox and HoloLens.

For companies willing to accept some risk, the cores could be ready to use in commercial chips within a year, according to

one engineer whose company is evaluating RISC-V and asked to remain anonymous. For more risk averse companies, it could take up to three years, he said.

In a sign of the breadth of interest in RISC-V, Oracle, who hosted the workshop in a theatre at its headquarters here, had six engineers signed up to attend the event including the vice president of Oracle Labs. Eight engineers signed up from AMD, the most from any one place except UC Berkeley which gave birth to the initiative in August 2014. Other attendees came from companies including ARM, Ceva, eASIC, Lattice, Huawei, IBM and Nvidia.

Google, HPE provide soft support

At the workshop, software experts from Google and Hewlett-Packard Enterprise (HPE) described work porting to RISC-V firmware stacks they are trying to establish as industry standards.

A Google engineer said the company has its Coreboot firmware already embedded in Chromebooks and Android-based TVs now running on RISC-V. He also called for help porting to RISC-V Google's Go programming language, a project a three-person team at Google has already started.

HPE has cobbled together a rough port of the UEFI firmware used in x86 PCs and servers. RISC-V lacks power management, trusted mode and systems management specifications, said Abner Chang, an HPE software engineer working on the UEFI port. Microsoft also needs to fill in key pieces of the UEFI port, he added.

Chang made a special plea for a management mode to enable the free core to achieve its full potential. "RISC-V is not just for embedded systems, we can bring it to PCs and servers," he said.

Another HPE engineer reported on a breakout group on defining the RISC-V memory model. "Memory subsystems are generally getting more complex…the feeling was there's a lot of work to be done in this space," he said, noting the potential to borrow many concepts established by x86 and ARM chips.

A separate security group parsed out a wide range of topics RISC-V could address. The effort has already attracted attention and support from both the U.S. and India governments for national security projects.

Draper Labs is developing a RISC-V chip using metadata to tag memory addresses with security policies, a concept developed in a secure computing program sponsored by DARPA last year.

In India, the Modi government has approved a budget that includes funding for a national microprocessor development project. Work could start as early as March when funding starts to flow to the effort that aims to create a family of RISC-V-based processors that would be available for military systems as well as commercial users in India.

A handful of papers presented projects using RISC-V as an embedded core in an FPGA that acts as an accelerator for various applications. For example, former Microsoft researcher Jan Gray described an FPGA using 400 RISC-V cores delivering nearly 100,000 Mips.

Gray's design, which he was able to boot on Christmas Eve, uses a novel network-on-chip with a compact router making it easier to place and communicate with cores in a large array. "This router will change the way people design large FPGAs," he claimed of the design he has yet to complete and aims to license.

Driving the agenda

President of Automotive Electronics at Bosch, Klaus Meder talks about how current trends in car design mean that tomorrow's vehicles will be fully internet connected, will run on renewable energy and will be increasingly autonomous…

Hanns Windele: What changes do you see arriving in the automotive electronics space? How will they affect Bosch as the biggest global automotive supplier?
Klaus Meder: I can see three major movements in the market, which I call: electrified, automated and connected. We can see today – and it will only increase over the next few years – that everything in the car is going to be electrified. Not only the powertrain, which is a whole story in itself, but literally everything. Take, for example, the steering system. This started out as completely mechanical, later with hydraulic assistance. Then it moved to a combination of electronics and hydraulics. Now, it is becoming purely electric, with the next step doing away with the steering column altogether, with no mechanical connection between the driver's hands and the wheels. Even in the compact class of cars there are now electric hatch doors, ventilation controls and so on.

President of Automotive Electronics at Bosch, Klaus Meder: "We want to be the 'integrated' IDM within Bosch to leverage vertical synergies"

Hanns Windele: And so the purpose of this is to increase automation?
Klaus Meder: If you want a future of partly-automated, fully-automated or autonomous cars, then you need to have all the functions electrified before you can start. You need to influence the steering, the powertrain, the lights and so on. If there are certain clearly defined conditions, such as a traffic jam, where the driver will be operating the vehicle 'hands off', you need every part of the car to be electrified in order to make it controllable. Without the electrification, automatic or even autonomous cars will not be possible.

Hanns Windele: Then there is connectivity?
Klaus Meder: This is the third trend that has been going on for some time now. Everything in the car is connected via the Controller Area Network CAN, FlexRay, Ethernet and so on. But now we have more and more connection to the outside over the air interface. First, the internet came into the car via the smartphone and the car became part of the internet. But now we will have direct connectivity between cars and infrastructure. There are already cars on the market that can download software over the air.

Hanns Windele: One of the key elements for these developments will be the increase in battery capacity and performance?
Klaus Meder: Our target is to double battery energy density and to halve the cost. So, we acquired the American battery company Seeo, which has solid-state technology and we think that they can meet the target. If we fulfill what we expect from the acquisition, it will be a very good investment.

Hanns Windele: You have an interesting collection of sensors on your windowsill?
Klaus Meder: Yes. I would actually donate this to a museum because it allows us to see the development of the technology since 1994. It started with a piezoelectric yaw rate sensor for the electronic stability control system (ESC) to prevent skidding of cars and so it saved a lot of lives. The sensors became smaller and cheaper as they became mass-produced and ended up in all cars in Europe and the US. So the technology evolved from being included in luxury cars, where you had to pay thousands of euros, to becoming a multidimensional very small MEMS sensor that is now in everyday gadgets, for example as a step counter or to control the screen direction. So it didn't just save thousands of lives, but it also made our lives easier.

Hanns Windele: Are you looking to investigate different markets?
Klaus Meder: The Automotive Electronics division of Bosch is involved not just in automotive, but also engaged in different markets where we find synergies for our technology and components. When we see such an opportunity, we are not shy to introduce 'speedboat' start-ups that can go very fast in their market. We founded Bosch Sensortec, which takes the technology we have developed for the automotive market into consumer electronics. Another example is our e-bike systems. We have also founded a company called Bosch Connected Devices and Solutions, where we are looking at sensors for the Internet of Things. Start-ups are very important because they bring in new ideas and have a fresh-eye approach. They are emotional and dynamic and can be a game-changer. We want to use this spirit in different ways: and so we are an investor, but we also have our own start-up culture with internal accelerators and incubators.

Hanns Windele: Do you think it is more difficult to do this in Germany than elsewhere?
Klaus Meder: Definitely. It's a case of mentality and availability of finance. It would improve things if we could change parts of our financing system – for example, allowing retirement funds to be invested in technology. That makes me sound critical. But actually, at the moment I am quite happy because three or four years ago we were saying that young people are not interested in working in technology – they only want to use it. Now, we see start-up

HANNS WINDELE is Vice President, Europe and India at Mentor Graphics. www.mentor.com

communities, such as the hub in Berlin, flourishing. There are others in Italy, Israel and India. So I think that young people are increasingly becoming more entrepreneurial and more technically oriented. This is a good thing for Bosch and the automotive industry. But maybe political leaders such as Angela Merkel and Francois Hollande could work on being more open-minded about technology and more positive in terms of encouraging young people into technology.

Investigating different markets with Bosch' e-bike systems.

Hanns Windele: Would you say that cross-functional development of technology is important to Bosch?
Klaus Meder: We are definitely a company that is driven by innovation in technology. We are on a journey to become more user-centric. The point of interest here for me is that you should not sell technology, but you should solve your customer's problem. Although I actually prefer the word 'user': the customer is the person who buys at the point-of-sale, and then there is the user, who will communicate with you their experience of the product. When you become more user-centric, you get very good success stories, such as the electric bike and the connected bike, where users are sharing their experience on-line and very quickly.

Hanns Windele: Is there one change in the market that would make this journey faster?
Klaus Meder: There are a lot of things that would make life easier, but in general what is needed is an improvement in quality systems. Quality is essential. No matter what the company size or location, this has to be unified and the target has to be zero defects. We have to become better at this. We have to improve quality and guarantee it.

Hanns Windele: What would help you to improve the quality of your electronics and chip design?
Klaus Meder: What we would like to have is an EDA system that is a seamless tool, from component layout up to system level. It should integrate analogue and digital, and we should be able to implement the test sequences and patterns in the same tool. Talking of quality, the tool should support standards such as ISO26262 for functional safety, and the tool should be qualified under this standard too. It should be fast, with no waiting times and then it should also have a very good human-machine interface. I have seen designers go crazy with frustration because the best tool is useless if you don't know how to use it. We are producing chips because we want to be the 'integrated' integrated device manufacturer within Bosch to leverage vertical synergies.

Hanns Windele: What will be the pace of electronic technology in automotive?
Klaus Meder: This is an important question. Because we are in the semiconductor industry, we all want to know how Moore's Law will continue. We can see already that it is slowing down: we are not doubling the transistor density every 18 months any more. It is more like every two or even two-and-a-half years now. We can also see that technology steps – like the 450mm wafer – are arriving later or being delayed. So we are seeing a tendency to slow down on the silicon base. But our whole industry relies on increasing functionality while decreasing cost – the so-called learning curve. We all depend on that: but now the question is whether the next technology will kick in early enough and fast enough to keep this trend on-going.

Hanns Windele: Is physical location any longer relevant to the automotive industry?
Klaus Meder: The rise of the Chinese market was an overwhelming development that most people didn't predict. I think there are many other markets that have the potential to develop in a similar way, such as ASEAN and Iran, or Russia. So I think that geography and geopolitical conditions matter for the development of the car markets. But when it comes to China, the whole of the industrial base is moving away from the image of being copycats, and their clear target is to become an important player in the field of technology too. Not only that, they will have the financial power to make it happen. China will also have the skills to do it. Therefore we will start to see their influence increasing.

Hanns Windele: In terms of environmental sustainability, what are the biggest challenges?
Klaus Meder: We need to make mobility environmentally acceptable and to have sustainable solutions. And it is important that we do this over the whole value-chain, starting with the manufacturing of the components, over the life span, right through until the recycling.

QUICKFIRE QUESTIONS

What's your idea of a dream holiday?
I like the oceans, so a nice hotel on a perfect beach with a new culture and cuisine to explore.

What are you reading at the moment?
Drive by Daniel H Pink, and I also like the mystery novels of Keigo Higashino.

What would you take with you to a desert island?
There's never enough food on small tropical islands. Also a toolbox.

If you could be the CEO of a non-tech company, what would that be?
A hotel. I'm fascinated by making the user experience better.

It there were extra hours in the day, how would you spend it?
More sports, definitely.

How many digital devices do you have on you just now?
One. My Fitbit Activity Tracker. My watch is analogue and my phone is on my desk.

What is the one gadget you couldn't live without?
A gadget is a gadget only because you can live without it.

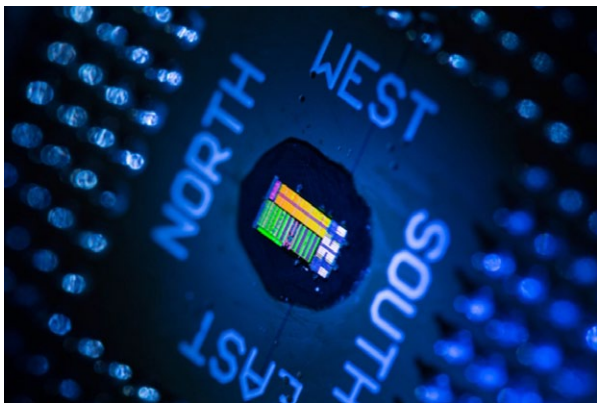
What piece of technology would you donate to a museum?
I would give my timeline of 20 years of automotive gyro components from my office.

Electro-photonic processor chip communicates directly by light

By Graham Prophet

In a letter to Nature, a group of researchers from University of California, Berkeley; Massachusetts Institute of Technology; and University of Colorado, Boulder, report the development of a highly-integrated photonic system comprising an IC that contains a processor, memory, and a large number of optical transceivers on a single die.

The development, described in a preview here, addresses the barriers presented to increasing bandwidths of inter-chip data communications by the physics of electrical signalling. Electrical SerDes interconnects have been extended far beyond what might once have been thought possible, but their limits may be in sight.



Optical solutions have been proposed for decades, but fabricating fully-integrated (monolithic) combinations of optical transceivers and current-generation logic has been challenging. Commercial suppliers such as the FPGA vendor Altera have proposed system-in-package solutions in which optical transceivers might be integrated as a separate die on a silicon substrate, tightly-coupled to logic dice (a.k.a. "2.5D integration") but no (open-market) product has yet emerged.

One of the issues that has limited such developments is the need to integrate optical emitters on the same process as the dense and fast logic; as well as the very different semiconductor process requirement, there are thermal and power issues to be resolved. The team reporting their results in Nature circumvent (some of) these issues by not having the light generated on the integrated substrate. Externally-generated laser light illuminates the die and data is transmitted by capturing some of that light, modulating it, and coupling the modulated light into a fibre.

The demonstration described verifies the capabilities of the optical link by using two identical chips; each contains a dual-core RISC-V processor core, 850 optical transceivers, and 1 MB of memory – over 70 million transistors in total. The tests described ran code on the core of one IC, but using the memory of the other, connected by optical links. A single laser source, via a power splitter, illuminated the ring-modulator transmitter on each chip, and the modulated light (via an optical amplifier) was routed to a receiver on the alternate chip. On each IC, the processor cores and the memory array each have their own, dedicated, set of electro-optic transceiver sites. The complete IC is 3x6mm in size.

In the test setup, fibre-positioners locate three (illumination/Rx/Tx) fibres over each chip. Fabrication using selective substrate removal enables controlled optical and electrical access to the Chip's resources.

Memory tests, and graphical rendering programs demonstrate that the optical link operates at zero BER. One observation that the researchers note is the sensitivity of the ring modulator to its thermal operating point, keeping it aligned to the laser light's wavelength; closed-loop on-chip heaters are required to stabilise the operating temperature and a shift of less than 1°C is sufficient to cause transmission errors to appear.

The research group adds, "...Instead of developing a custom process to enable the fabrication of photonics, which would complicate or eliminate the possibility of integration with state-of-the-art transistors at large scale and at high yield, we design optical devices using a standard microelectronics foundry process that is used for modern microprocessors. This demonstration could represent the beginning of an era of chip-scale electronic–photonic systems with the potential to transform computing system architectures, enabling more powerful computers, from network infrastructure to data centres and supercomputers."

18-inch rollable display showcases future potential of OLEDs

By Paul Buckley

LG Display has showcased a number of futuristic concept displays at CES 2016 that highlight the dynamic forms that OLED technology can achieve. One innovation includes the world's first 30R 18-inch rollable display that can be rolled-up like a newspaper.

The South Korean company also revealed a 55-inch design concept OLED TV display that is paper-thin because the device's electric circuits are installed separately; and a matching pair of 65-inch extreme-curve concave/convex OLED displays.

LG Display also exhibited 65-inch and 77-inch UHD OLED TV panels that claim to offer the ultimate picture performance in terms of contrast, color accuracy, and viewing angle. The 65-inch and 77-inch OLED TV panels, featuring a High Dynamic Range (HDR) function with its perfect black and improved luminance, claim to provide unbeatable picture quality and the same level of color gamut seen in professional monitors used to edit theatrical films.

The company is highlighting OLED's potential in the commercial sector by introducing a 55-inch double-sided display which shows different video images on each side for signage and a 139-inch Vertical Tiling OLED (VTO) display that is made of eight double-sided 65-inch OLED panels that are connected together to form a S-shape pattern. This VTO display also shows different video images on each side.

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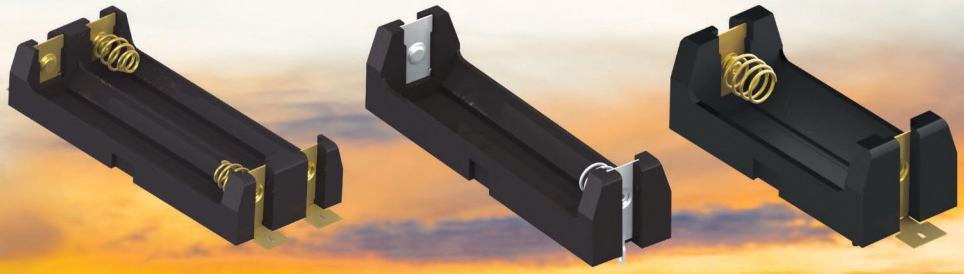

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Hublex: a custom fit for industrial mobility

By Julien Happich

With its slim and lightweight hub-less gyropod, French startup Hublex is onto something big, so to speak, looking at a market potentially much bigger than what Segway was ever able to serve with its comparatively cumbersome individual transport solution. Interestingly enough, the French hub-less implementation finds its origins in a thorough teardown of a Segway gyropod at the IUT of Cachan (University Institute of Technology in Cachan, France). The teardown triggered enough interest from students and professors to make them want to build their own version, with ingenious simplifications.

But hasn't Segway carefully protected its inventions? "Yes it has", concedes Jonathan Lévy, Hublex' CEO. "But patents only last for 20 years, the first Segways were conceived 23 years ago and all the IP relating to these self-balancing gyropods, the control algorithms in particular, have been in the public domain for the last three years".

As a university project led by professor Pascal Martinelli (now Hublex' scientific supervisor), mechanical and electronic engineering students set to investigate a better way to build their own gyropod. In particular, something lightweight and truly portable that they could use to wiz around on the campus (the original Segway weighs about 60kg and can't be easily lifted upstairs).

Ensued five years of research and development which yielded a gyropod with roughly half the footprint, only 38cm wide, and weighing a fifth (12kg), while offering better performances and higher reliability, mobility-wise, at a fraction of the price of Segways.

"The teardown revealed there were many mechanical parts just for motor reduction, and a lot of complex electronics associated with it. We found about 2000 part references, whereas our solution now only has about 45 references", explained Lévy, admitting that electronics and technology has come a long way in 20 years.

The most innovative part of the Hublex is its electric motor configuration (one for each wheel), with the axis sitting directly in contact with the internal circumference of the wheels' rims. The rims are driven by friction, they also act as the gear reduction mechanism (you only need to run the motor faster to increase speed to your liking).

The motors' axles directly sit on the internal rim of the hub-less wheels.

Hublex' CEO Jonathan Levy, stepping on a working prototype.

This configuration also self-centres the wheels and lowers the platform.

"With this arrangement, we can benefit from a natural x10 to x15 gear reduction (depending on wheel size) while greatly reducing weight. Also this allows the platform to be only 10cm off the ground, compared to 25cm for the Segways. This means you don't need to wear a helmet to prevent knocking yourself out accidentally on a door frame" explains Lévy.

But that's not all. The control handle has been designed as a lightweight and removable mechanical joystick (for easier packaging), situating the gyropod's centre of gravity below the wheels' axis, hence it is self-balanced even in the off-mode (as long as you don't step on it).

Lévy is aiming the new gyropod at the industrial B2B market, for maintenance, security and emergency staff on large sites where either walking long distances or driving a car is counter-productive.

"All our prospective clients use or have used Segways, but they soon realized their limitations.

One particular limiting factor is their weight and width. We worked with prospective clients such as Aéroports de Paris and Alcatel Lucent and one requisite was that the gyropod should not be wider than 40cm to be carried up narrow staircases on industrial sites or to use escalators, because of the bollards that limit their access in most airports".

According to Lévy, the weight (non-portability) and width limitations of Segways make the running costs escalate, as industrial sites now need to provision individual units for each floor level to be accessed. The fleet may also be doubled just for the sake of availability, during battery charge times. According to the CEO, Segways was more focused on the B2C market, hoping to serve all purposes at once (commuting, recreational, industrial use) by pushing a product without really investigating into the specific requirements of each market.

"Our specific battery design ensures 24/7 availability of the gyropod. And because our solution is lightweight and more energy efficient, we can use proven NiMH technology which is more rugged than Li-ion batteries and can be safely shipped or stocked" completes Lévy.

Starting in January and February 2016, the startup will run a pilot trial at Aeroport de Paris, with between 7 and 10 vehicles shared across 55 users with different profiles and responsibilities. With over a 100 Hublex already pre-ordered, the CEO is confident it will get the funding to bring its gyropod to full scale production.

The final R&D project was recently funded by SATT Paris-Saclay (a local technology transfer accelerator) for an amount of 300,000 euros. While the IP and patents belong to Université Paris-Sud, Hublex has exclusive licensing rights to industrialize the technology. In exchange of its investment, SATT Paris-Saclay will get a cut of the royalties.

Hublex is now actively looking for investors to finalize the industrial and commercial development of its gyropod, hoping to secure one million euros within the next six months. For industrial use cases, Lévy thinks a leasing business model will be more attractive, offering 24/7 maintenance services as a package to large sites.

The CEO ambitions to become the European leader of personal electromobility for the last mile on industrial estates, with gyropods manufactured in France.

Five to six years down the line, Lévy hopes to enter the stock market and possibly expand its offering to consumers to grow beyond industrial markets, possibly with a lighter version just under 10 kg.

Beyond electromobility, Hublex' ingenious motor configuration could find use cases in robotics, potentially displacing many 3-wheeled implementations. The motor itself was custom designed and built so to withstand high radial loads (the Hublex is qualified to support 120kg), so in the future, the motors alone may justify a new line of business for the company.

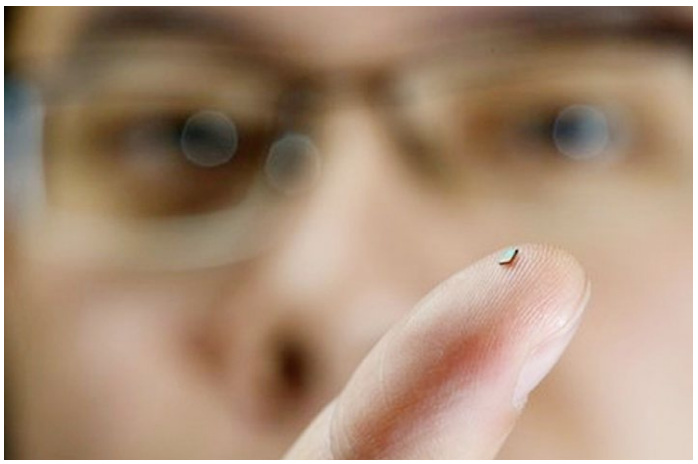
Radio powers autonomous temperature sensor

By Peter Clarke

Researchers at the Technical University of Eindhoven have developed a wireless temperature sensor that is powered by millimeter wavelength radio waves that are also used for communications.

Eindhoven student Hao Gao was due to receive a Ph.D. earlier this month for his thesis in which he discusses his development of the sensor that has an area of 2 square millimeters and weighs 1.6mg. The sensor is made using a 65nm CMOS manufacturing process.

A specially developed wireless router communicates with the sensor, which has an antenna on chip and picks up both energy and information from the millimeter wave signals. The current version of the sensor has a range of 2.5cm but researchers hope to extend this to a meter within a year. The autonomous nature of the temperature sensor means it can be put behind plasterboard or included in a screed of concrete or paint



Temperature sensor on the finger of PhD-student Hao Gao. Photo: Bart van Overbeeke. Source: Technical University of Eindhoven.

The sensor stores the energy received and once there is enough switches on, measures the temperature and sends a signal to the router. Each temperature is indicated by a slightly different frequency at which the return signal can be sent. The router determines the temperature by the distinctive frequency.

The same technology could be used with other sensor types, such as motion, light and humidity. The tiny size of the silicon chip is expected to keep sensor costs down to around 20 cents in volume.

The title of Hao Gao's thesis is Fully Integrated Ultra-Low Power mm-Wave Wireless Sensor Design Methods. The IC research was done in the Mixed-Signal Microelectronics group and also involved university groups specialised in electromagnetics and signal processing systems as well as the Center of Wireless Technology.

Software-upgradable cars launch new platform race

By Junko Yoshida

Software over-the-air upgrades for cars are the next big thing in automotive electronics. But which hardware platforms will enable carmakers to implement the desired feature? Nvidia, NXP and Renesas appear to have diverging strategies.

There is little argument that Tesla Motors changed the conversation around automobiles in 2015, or that NVidia caught a ride on Tesla's coattails. Tesla has set the stage for the automotive future by rolling out new autopilot features — such as lane keeping and self-parking — via over-the-air (OTA) software upgrades. Tesla showed a glimpse of the future in which consumers don't need to buy a new car to add features.

The presumptive car of tomorrow, behaving like a smartphone, is software upgradable. Of course, OTA isn't a foreign concept to the automotive industry. Some car makers like Nissan have been sending software patches over the air. Ford is partnering with Microsoft to provide continual updates to its next-generation infotainment systems.

But none of the automakers has added software upgradable features for engines, transmissions, brakes or suspensions — like what Tesla did in enabling some autonomous driving functions via software.

Changing conversation

To put it mildly, Tesla is freaking out car OEMs and Tier Ones. Today, none of the conventional carmakers can offer anything close to what Tesla does — "without changing the entire hardware and software architecture in a car," explained Danny Shapiro, Nvidia's senior director of Automotive.

Armed with the company's DRIVE PX platform based on its own Tegra X1 processor, Nvidia is coming to Las Vegas for CES, pitching its centralized CPU platform to "make cars better and improve their value," Shapiro explained.

Acknowledging Tesla's halo effect, Jeff Bier, founder of the Embedded Vision Alliance, said that software upgrades "will create huge opportunities — to save people's lives and improve efficiency."

Nvidia, a relative newcomer to the automotive field, has nothing to lose in prompting carmakers to start from scratch and embrace a brand new centralized CPU platform like its PX platform for their new models.

In contrast, neither NXP nor Renesas Electronics – two leading automotive chip suppliers – can afford a grandstand move like Nvidia's. A lot of their chips are already designed into millions of cars.

Digital networking processor inside a car

In an interview with *EE Times*, Kurt Sievers, executive vice president and general manager of NXP's automotive business unit, said, "Nvidia certainly knows how to speak high-tech language" that gets people's attention.

A modern car already deploys more than 50 ECUs inside a vehicle, with each tasked to dedicated functions, much like a distributed computing architecture.

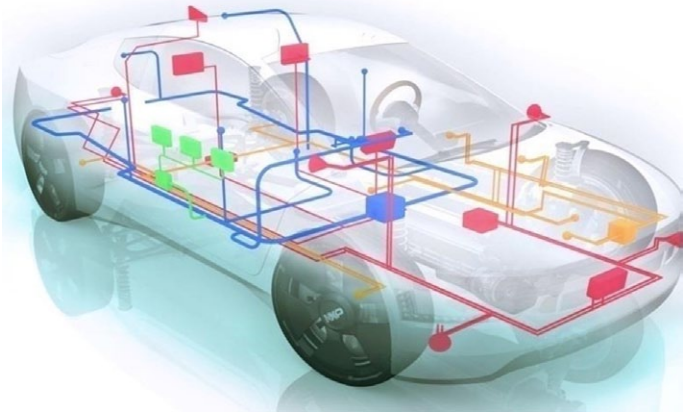
Since modern cars use many sensors, each ECU also has to pre-process sensory data, which needs to travel via secure connections to a central processing unit for sensor fusion, explained Sievers. Fully aware of the need for a powerful platform to perform software upgrades and complex sensor fusion, NXP, freshly merged with Freescale, is offering car OEMs high-performance multicore networking processors — originally developed by Freescale's digital networking group. "We are letting our customers try these samples," explained Sievers.

Sievers, however, does not agree with Nvidia's approach, which is reminiscent of Intel's brute-force CPU-centric push for PC improvements. Nvidia today makes no bones about leveraging sheer processing power to revolutionize vehicle architecture and improve the car's capacity for deep learning.

Nvidia is applying its GPU-accelerated deep learning expertise to computer vision. In medicine, for example, the same technology is used to detect cancer cells, said Shapiro. "Frankly, if your only application is automotive, I don't think you can match the resources you need to explore deep learning as the way we've been able to do."

Focus on security

NXP believes that to increase the reliability of cars, it needs to go beyond a powerful CPU-based platform and offer much more secure vehicle network architecture. To that end, NXP is beefing up security throughout the in-vehicle network where critical data travels, explained Sievers.



NXP is putting a tamper-resistant, secure hardware element — akin to a front-door lock — in each interface where external data enters a car via Bluetooth, cellular or V2V connectivity. If the data's source can't be verified, the hardware element can shut it down.

The next issue is the data that floats around inside the vehicle network. "It's like securing corridors inside a house," said Sievers. This is easier said than done because the in-vehicle network's domain structures include a number of branches. Without detailing how NXP plans to secure this network, Sievers said, "We have some ideas. We're working on it right now." Once the data reaches applications – "similar to getting inside a room at home," Sievers said, "We will run security in software."

Protecting vehicles from hackers takes complex planning and execution. Egil Juliussen, director research, Infotainment &

ADAS at IHS Automotive, observed that "hacking research has shown that nearly all access points can be compromised."

Can you undo changes?

Amrit Vivekanand, vice president of automotive business for Renesas Electronics America, singled out "OTA software upgrades" as one of the biggest industry challenges. While attendees at the CES 2016 will see many enabling technologies for autonomous cars and V2V car communications, he said, OTA remains a huge deal for automakers. "There is no consensus on how to achieve necessary levels of security, memory, processors and gateways" for software upgradeable cars, said Vivekanand.

In adding new automotive features via software upgrades, engineers worry about the security of the operation, robustness of the technology, and resources available inside a car, he explained.

Sure, you can download your software upgrade. But what if the upgrades don't work? In particular, Vivekanand wonders, "How do you undo changes? Can your car revert back to the state before you did the upgrade?"

The "undo" imperative presents an interesting challenge to vehicle designers. "Do you double the size of a flash memory or add another bank of memory that can store the original state before the upgrade?" Neither is cheap, said Vivekanand. But if the car can't do certain software upgrades, shouldn't it just warn users that the current version 2.0 platform in this vehicle is too pooped to pop? "In theory, yes," said Vivekanand. "But when a number of modules are due for software upgrades at the same time, there is always a risk that some software upgrades can go wrong." This applies especially to software upgrades in different modules that aren't pre-tested together.

Assume, for example, you're trying to upgrade HVAC (heating, ventilation, and air conditioning) software. But the updates don't kick in. Vivekanand said, "Consumers will ask for an undo command button." The car should ask the driver to turn off and turn on the car — a classic reboot manoeuver that would restore the original HVAC state in 5-10 seconds, he explained.

ASIL B to ASILD

Renesas, earlier this month, launched R-Car H3, dubbed the "first SoC from the third-generation R-Car automotive computing platform for the autonomous-driving era." The new R-Car H3 features improved computing performance and automotive functional safety support, claimed Renesas. The R-Car H3 is built around the ARM Cortex-A57/A53 cores, employing the newest 64-bit CPU core architecture from ARM.

The on-chip IMP-X5 parallel programmable engine offers advanced image recognition technology in addition to the CPU and GPU. The IMP-X5, exclusive to Renesas, is "a recognition engine that is optimized for interoperation with the CPU," the company said. While the R-Car H3 is already compliant to ISO 26262 (ASIL-B), Renesas' Vivekanand said that the company's plan is to offer even higher functional safety on its autonomous car platform. Renesas is adding, in a module, its PH850/P1X microcontroller — which can offer a "lockstep core for CPU."

The PH850/PX1, designed for controlling the chassis, steering and braking, can be used to validate R-Car H3 output, by running similar calculations and defining the boundaries, explained Vivekanand. The R-Car H3/PX1 combined module, which improves its functional safety further to ASIL-D, can tell the car what to do via real-time communication, he added.

Harman demos pupil-based driver monitoring system

By Christoph Hammerschmidt

Driving while distracted or tired is one of the most significant factors that eventually lead to fatal traffic accidents. With a system that constantly monitors the driver's pupils, automotive supplier Harman hopes to enable the design of driver assistance systems that reliably prevent such accidents.

Harman's system, demonstrated at the Consumer Electronics Show (CES) in Las Vegas, measures increases in pupil dilation as an indication of a driver's mental workload. Most available systems for this purpose measure the driver's steering movements and detect slight erratic irregularities triggered by a lack of driver's attention.

While there have been approaches that monitor the driver's eye movements before, Harman has developed a new proprietary eye and pupil tracking system that, according to the company, measures high cognitive load and mental multitasking in the driver's seat, and signals the car's other safety systems to adapt to the driver's state. The company believes that its technology represents a major step forward in the domain of Advanced Safety and Driver Monitoring Systems (DMS) for vehicles.

Adoption of in-cabin cameras is growing rapidly, enabling features such as occupant detection and driver drowsiness monitoring. With the introduction of high cognitive load detection, Harman's eye and pupil tracking technology brings additional value to the driver-facing camera in that the technology eliminates the need for complex sensors built into seats and steering wheels, or biometric sensors that require physical contact with the driver.

An algorithm analyses the pupil reflex using advanced filtering and signal processing. The filter isolates and identifies responses triggered by high cognitive load. The calculated outputs are used to intuitively adjust user interfaces, like placing mobile devices in do-not-disturb mode or adjusting ADAS system intervention thresholds to minimize physical and mental distraction to the driver.

Facebook preps Open GPU server

By Rick Merritt

Facebook will make open source a GPU server geared for machine learning. Big Sur packs eight Nvidia Tesla M40 graphics accelerators, each drawing up to 300 watts, and is the first system to use the high-end cards targeted at training deep neural networks.

The work is one of many efforts to apply FPGAs and GPUs to accelerate big data center jobs, increasingly using deep neural networks. More than a year ago rivals Baidu and Microsoft said they were rolling out FPGAs for a variety of data center applications including search, claiming GPUs have greater performance but at much higher power consumption and cost.

In February, rivals Microsoft and Google announced breakthroughs in image recognition using deep neural networks. Big Sur marks Facebook's first foray beyond standard server, storage and switch designs. In November, Facebook announced a 100 Gbit/second switch.

Details of Big Sur won't be available until an unspecified date when the design is released to the Open Compute Project, originally launched by Facebook. However, the Web giant did say the server uses the project's Open Rack specification. In addition, it has "flexibility to configure between multiple PCI-e topologies."

Facebook's artificial intelligence research team is only working with Nvidia for now. Big Sur "was built with the Nvidia Tesla M40 in mind, but is qualified to support a wide range of PCI-e cards," said a Facebook representative.

Nvidia was chosen for a variety of reasons, including the "fact that they have hardware agnostic APIs like Open CL," the Facebook representative said.

Big Sur packs eight Nvidia Tesla M40 accelerators using an OpenCL interface, but is qualified to handle other PCI Express cards. (Image: Facebook)

Facebook is currently in the final phase of testing Big Sur with plans to use it in production networks next year. The Web giant has "developed software that can read stories, answer questions about scenes, play games and even learn unspecified tasks through observing some examples. But we realized that truly tackling these problems at scale would require us to design our own systems," engineers said in a blog.

Facebook would not say how much it has invested in researching the field of machine learning or building the GPU server effort. However it did say the group "is more than tripling its investment in GPU hardware as we focus even more on research and enable other teams across the company to use neural networks in our products and services."

Facebook is currently using off-the-shelf GPU servers to handle machine learning tasks, but they require special cooling, are relatively expensive and are difficult to maintain, the blog said. Big Sur can be air-cooled like other systems in Facebook's data centers

As with other servers optimized for big data center operators, Facebook streamlined existing designs to save cost and ease maintenance. "We've removed the components that don't get used very much, and components that fail relatively frequently — such as hard drives and DIMMs — can now be removed and replaced in a few wseconds," the blog said.

For example, the Big Sur motherboard can be removed in a minute, compared to an hour's work for existing GPU servers. The CPU heat sinks are the only replaceable items in the design that require a screwdriver, it added.

Apple pays to settle with Ericsson

By Peter Clarke

Apple and Ericsson have agreed a global cross-license for patents essential to the GSM, UMTS and LTE cellular standards and granted certain other patent rights to each other, settling a long-standing dispute.

The two companies also plan to collaborate on 5G communications, video network traffic management and wireless network optimization.

The terms of the seven-year deal were not disclosed but Apple is making an initial payment and will pay on-going royalties to Ericsson. Ericsson said that taking into account the Apple payments and other royalty bearing licenses its IP business would be worth between 13 and 14 billion Swedish Krone (between $1.54 billion and $1.65 billion) in 2015.

The agreement puts an end to law suits pending in Texas, California, the United Kingdom, Germany and the Netherlands and also ends an investigation being conducted by the U.S. International Trade Commission.

DARPA funds atoms-to-products breakthrough

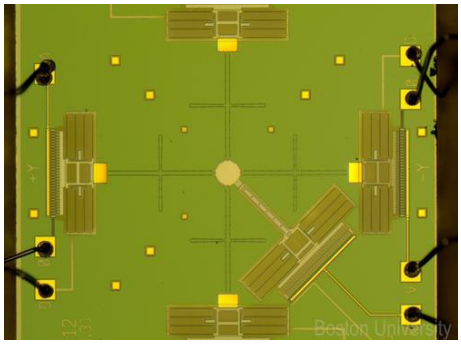
By R. Colin Johnson

Materials have uncommon electrical and quantum-level properties at the nanoscale that disappear at the millimeter-scale, where most chips are manufactured. The Defense Advanced Research Project Agency (DARPA) is looking for a way to capture the benefits of both worlds: the nanoscale manufacturing while upsizing to a more practical millimeter scale. The agency has now set that challenge to 10 laboratories nationwide in its Atoms to Products program.

"These 'atomic-scale' behaviors have potentially important defense applications," says DARPA's Atoms to Products website, "including quantized current-voltage behaviour, dramatically lower melting points and significantly higher specific heats, for example. The challenge is how to retain the characteristics of materials at the atomic scale in much larger 'product-scale' (typically a few centimetres) devices and systems."

One of the leading contractors, HRL Laboratories, LLC (Malibu, Calif.), spoke about the program to EE Times last October, before DARPA was ready to go public with some aspects of the program. HRl has subcontracted with Intelligent Materials Solutions (Princeton, New Jersey) to extend the nanoscale magic of advanced materials by precisely assembling them atom-per-atom.

"To get the benefits of nanoscale engineering at the millimetre scale, we partnered with Intelligent Material Solutions," said team leader Adam Gross who is working with Christopher Roper to realize the Atoms-to-Products dream. "Our initial project will be to control infrared light by assembling nanoscale particles into finished components that are one million times larger."



Boston University's microscopic tool called a nanoscale "atom writer" fabricates minuscule light-manipulating structures on surfaces. (SOURCE: Boston University)

Current nanoscale fabrication techniques are subtractive, such as photolithography, etching and vacuum deposit, but by assembling three-dimensional (3-D) structures--atom-by-atom--HRL and Intelligent Material Solutions hope to extend the amazing quantum effects realized at the nanoscale to chips at the millimetre scale.

"We have already shown we can assemble two types of nanoparticles for the control of infrared light," said Gross. "We assemble layer-upon-layer of spherical diffraction gratings. Our first milestone will be to assemble two types of sub-200 nanometre gratings into 210 micron assemblies that maintain their nanoscale properties."

That step will take 12 months of the 3-year program. The second step will be to assemble those micro-scale subassemblies into millimetre-sized products that continue to maintain the quantum effects, as well as the lower melting points and higher specific heats of nanoscale assemblies.

Other participants, more ideas

Nine other teams working on different projects, including medical applications. The other teams include: Boston University, Draper Laboratory (Cambridge, Mass.), Embody (Norfolk, Virginia), Harvard University (Cambridge, Mass.), SRI (Menlo Park, California), the University of Notre Dame (South Bend, Indiana), Voxtel (Beaverton, Oregon), Xerox Palo Alto Research Center Inc. (PARC, California),and Zyvex Labs (Richardson, Texas).

Embody will concentrate on developing collagen nano fibers that can mimic natural ligaments to the medical recovery of soldiers for quicker and 50 percent lower cost that today. And as with all DARPA programs, they hope that their success will seep into the civilian world of sports injuries.

Draper will concentrate of radio frequency subsystems to boost their range and global positioning accuracy by 20 times by assembling nanoscale braiding subassemblies first at the micron scale then finally at the millimetre scale in phase two. Their technique will be to copy how DNA self-assemblies into an intertwined structure.

Voxtel and Oregon State University will concentrate on imitating nature's ability to self-assembly multi-material structures using high-rate fluid-based processes by combining the synthesis and delivery of materials to inkjet-like three-dimensional (3-D) mixed organ and inorganic materials which retain the best qualities of both at a price lower than either alone.

Boston University will aim to build atomic-scale calligraphy techniques that can "spray-paint" with atomic accuracy for tuneable optical metamaterials built on the 'photonic" battlefield.

The University of Notre Dame will aim for parallel nano manufacturing techniques that enable optical metamaterials to be manufactured on-demand with specific 'designer' characteristics. Their technique will use optical tiles that can quickly assembled in different configurations using single-atom electrochemistry.

Xerox PARC is creating the world's first digital micro-assembly printer using micrometre-sized ink particles that can assembly centimetre-scale assemblies that maintains nanoscale properties for secure communications, surveillance and electronic warfare.

Zyvex is hoping to create microscale devices with nanoscale properties from the top-down and with atomic precision for ultra-sensitive sensors, threat detection, quantum communications and sand-grain sized atomic clocks.

SRI is aiming to create what it called "levitating micro-factories" that combine micro-electro-mechanical systems (MEMS) with pick-and-pace robot "swarms" that connect micro-scale subassemblies with nanoscale properties into millimetre-sized products ready for deployment.

Harvard is creating a new era of millimetre-scale surgical tools 2D layer-by-layer composition processes to create complex meso-scale 3D devices for specific surgical procedures. Their goal is to allow surgeons to retain tactile feedback even when performing micron-scale surgeries.

French startup plugs smartglasses into bikers' helmets

By Julien Happich

As you would suspect, the 2015 Paris Motorcycle Show held Portes de Versailles was, well, full of shiny motorbikes. But one exhibit that really caught my sight was the in-retina display plug-in helmet accessory that Eye-Lights co-founders Romain Duflot (CEO) and Thomas De Saintignon (CTO) were demonstrating at the www.motoblouz.com stand.

The duo of freshly graduated engineers from ICAM Toulouse (mid-2015) developed and prototyped their Moto Display helmet add-on over the course of their last year as students, "the company is being registered as we speak" explained Duflot Romain.

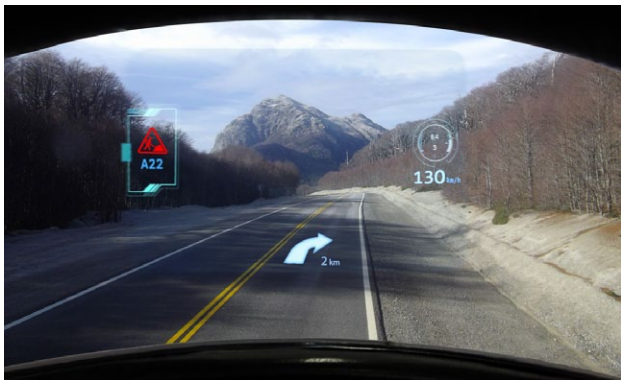
The Moto Display comprises of a clip-on image projection and lens unit which is fed data from a lightweight Bluetooth-enabled module that sticks to the helmet. "What you see is only a prototype", insists Duflot. Indeed, most if not all of the mechanical parts are 3D printed from plastic.

The Bluetooth connection retrieves GPS and mapping data from the biker's smartphone, a dedicated application turns the data into clear traffic instructions displayed as a virtual images forming directly onto the wearer's retina, as if seen at a distance. The beauty is that you always look in front of you, not in any tiny corner like it would be the case with the Google glasses, so you keep the road and traffic in sight while your speed and guiding arrows are floating in a distance.

But this has been done before, hasn't it? Or at least something similar but fully integrated, look at the Skully AR fully integrated smart helmet, a real success on Indiegogo. So why not go for a full integration?

Eye-Lights' CTO De Saintignon wouldn't want to discredit competition, yet he hinted that the helmet quality may not be up to the best standards. "As a tech company, we'd rather focus on the added-value our technology can bring and offer it directly to consumers than improvise ourselves helmet manufacturers".

"What's more, because the device is an add-on, just any one owning a helmet can use it. You don't have to depart from your favourite helmet and buy another one that may not match your taste or your look", added Duflot, "a helmet is a very personal item, and many bikers would be reluctant to change theirs".



Indeed, looking at it this way, the potential market for the Moto Display is much larger, and it could serve use cases beyond regular bikers (law enforcement or emergencies). Just think about automated licence plate-recognition from a built-in front camera on a police motorbike, coupled with an eye-level alert whenever the agent crosses path with a wanted plate-number.

Anyhow, reaching consumers is on Eye-Lights' priority list. The company is currently looking for investors to help them finance further product development and to strike deals with future manufacturing partners. "Within a year or so, we'll probably be ready to make our public product launch through a crowd-funding campaign, but before, we must be 100% sure about our production costs. In such a project, a Kickstarter campaign is only the emerging tip of the iceberg, there is a lot of work to be done before" Duflot concluded.

Now, if such add-ons were to become popular in the future, wouldn't helmet manufacturers want to integrate most of the recurring electronics, say a battery compartment and a small board with a Bluetooth connection, seamlessly designed somewhere at the back, and a couple of versatile outputs near the visor for most gadgets to plug in?

Not really. Most helmet manufacturers at the show would say their highest priority is the wearer's protection and comfort, which according to most of them, is in contradiction with any inclusion of electronic hardware. They consider electronics as dead weight, extra grams that would invariably alter the comfort and that would make their offering compare unfavourably with their competitors' products.

But what if augmented reality became a must-have for helmets? Managing director for Arai Helmet Europe, Ingmar Stroeven admits he has seen study prototypes, tentatively designed as conceptual products from automotive business partners.

But from Arai's standpoint, these helmets would never pass the stringent reliability and safety tests at the level that makes the company's helmets stand above the crowd. "Passing the ECE mark is one thing, and many helmets do just that, but we build helmets that go beyond basic ECE standard protection."

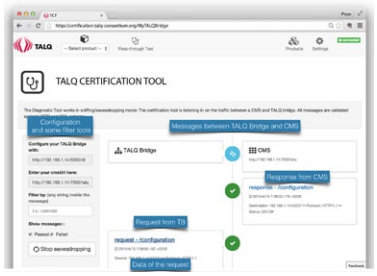
"I've seen a head-up display helmet prototype, but it was not convincing enough and at Arai, we would never build anything into our helmets that would not either directly improve comfort or increase protection. Today's electronics is too cumbersome. It would have to be really tiny and weigh literally nothing before we would consider integrating electronics", concluded Stroeven.

Global standard for outdoor lighting control

By Paul Buckley

The TALQ Consortium, which is aiming to develop a global standard for interfaces to manage outdoor lighting networks, has made a step towards the official rollout of the TALQ Certification Program.

During the first TALQ plug fest in Valencia, Spain, the specially developed Test Tool to be used to test outdoor lighting products for TALQ-compliance, was successfully applied with various control technology implementations. Several central management and TALQ bridge systems were also tested for compatibility against each other. The results confirm that the test procedures are nearly ready for the launch of the Certification Program.



One important factor for cities and communities on their way to becoming a 'Smart City' is street lighting. Because road lighting on one hand has a huge impact on the safety and quality of life in a city, and on the other hand requires a significant spend on energy and maintenance for a smooth operation. For all entities maintaining outdoor lighting networks there are three key factors. Firstly, they want to build up future-proof systems, because investments have to prove their suitability for decades. Secondly, they want intelligent platforms to guarantee efficiency and flexibility in operation. And, last but not least, they do not wish to be tied to a single supplier but prefer a sound competition and strive for compatibility between components of different vendors.

To support all of these market needs, the TALQ Consortium, an open initiative composed of leading lighting industry players, is working on setting a global standard for the interface to control and monitor diverse outdoor lighting networks (OLNs).

In 2012 the members started to develop the TALQ Specification which focuses on the so-called 'application layer' of the interface protocol, thereby allowing maximum freedom for manufacturers to develop optimized solutions within an interoperable framework. The TALQ Interface is built on standard internet protocols and security standards, such as XML/HTTP and Transport Layer Security, and is independent of connectivity technology.

To assure the highest level of security and error-free interoperability a rigorous test procedure and test tool were also developed. The TALQ Test Tool itself and several products of members were put to the test in Valencia, Spain, during the first week of December 2015.

"We were able to test each one against all the other corresponding products. On the final day we saw one central management system successfully controlling two other TALQ bridge products concurrently, all from different manufacturers." reported Dr Nick Hewish, Test Tool Development Supervisor of the TALQ Certification Workgroup, about the recent plug fest sessions.

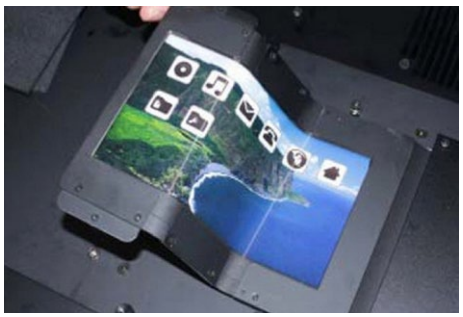
Apple has moved into former Qualcomm display lab

By Peter Clarke

Apple has started work in a small-scale production facility in Longtan near Taipei, Taiwan on display technologies, according to a Bloomberg report.

Apple moved into the facility in April 2015 and has at least 50 staff employed there on developing display technology for mobile devices including iPads and iPhones, the report said. The facility had previously been occupied by Qualcomm Panel Manufacturing Ltd. and was one of the places where Qualcomm tried to develop its Mirasol, moving-MEMS display.

However, the Mirasol display was not a success because, although it was non-volatile and therefore energy efficient and reflective and therefore daylight readable, it was less vivid than backlight LCD or OLED displays.



Triptych 5.9-inch AMOLED display. Source: Japanese research institute Semiconductor Energy

Apple currently uses back-lit LCDs in its equipment supplied by such companies as Sharp Samsung and Japan Display but is expected to move towards OLED displays, a move already taken by Samsung in mobile devices and by TV makers. Samsung has already introduced flexible OLED screens and foldable and rollable screens are considered a next development.

Apple could be using the facility at Longtan to develop its own OLED manufacturing processes for displays that it could then outsource to local Taiwanese manufacturing companies such as AU Optronics and Innolux Corp. This would reduce its dependence on companies such as Samsung who might otherwise control and limit Apple's access to the latest technologies.

Apple is increasingly pulling component and subsystem engineering in-house as evidenced by the news it has bought a small-volume 200mm wafer fab in Silicon Valley.

It is unlikely that Apple has done more than taken over a building previously occupied by Qualcomm although Qualcomm has previously said it would seek licensees for its Mirasol technology.

Mirasol dates back to before 2004 when Qualcomm paid $170 million for startup company Iridigm Display Corp., which originally developed the technology. Back in 2012 the company pulled back from using its Mirasol display and said it would seek licensees for the technology. But with no further announcements it seemed that Mirasol would join a number of other display technologies as an engineering curiousity but commercial failure. A Mirasol display was used in the Toq, a proof-of-concept smartwatch that Qualcomm released in December 2013, but this smartwatch was itself not a conspicuous success.

Can prime-time charging of EVs reduce smart grid crunch?

By Paul Buckley

Researchers at the Norwegian University of Science and Technology (NTNU) are helping to develop smart grid solutions that aim to ease the crunch caused by powering our transportation with electricity.

When people with EVs come home from work in the afternoon, they plug in their cars to charge them. That results in an extra peak in electricity consumption in the afternoon.

"We're moving towards a different kind of power use," suggested Professor Olav B. Fosso, professor and director of the Energy strategic research area at the Norwegian University of Science and Technology (NTNU). This peak may eventually become a major challenge for the electrical grid.

"We could have big voltage problems, with limited transmission capacity within the distribution system," explained Fosso.

Capacity could also become a problem. Large variations in consumption throughout the day are challenging. Electrical power is perishable which means it is an advantage to have relatively stable power use over a 24-hour period. Renewable energy from the wind and sun has to be used immediately.

Fosso admits Norway is lucky to be able to regulate its hydropower. Water reservoirs allow adjustments in the power supply, but few countries have that ability, and even in Norway high consumption at certain times of the day poses a challenge.

Afternoon charging of electric cars is not a problem — yet. But the orders for electric cars in Norway show that growth will not stop with the almost 75,000 EVs already on the road, including hybrids.

"Nothing suggests that this development won't continue," said Fosso.

Cars have different charging power and storage capacities. Storage capacity is related to the car's range. Mitsubishi's capacity is around 16 kWh, while the Nissan Leaf has a capacity of around 20 kWh and Tesla, 85 kWh. Battery size determines the charging time for a given amperage, with typical charging efficiency ranging from 4-8 kW. Home chargers provide long charging times, but that may become problematic when a lot of people charge their cars at the same time in residential areas. Quick charger installations require a higher current feed and thus a stronger electrical grid.

Fast chargers of around 20 kW are now available for home use in the United States. If this type of rapid charger becomes more common in Norway, so will problems.

Afternoon peaks in power use are common, because people come home and turn on heaters and appliances. But this peak will also be increased when people come home and plug in their EVs.

That is when people have to get smart in how they use the power. A Smart Grid - which uses new technology to better leverage the electrical grid - will likely be an essential part of the solution.

NTNU's Faculty of Information Technology, Mathematics and Electrical Engineering (IME) is involved in developing a Smart Grid in Norway and its research will have a direct effect on consumers' electricity bills.

At the moment, when consumers get an electricity bill, they pay it and probably do not think about it again, since they might have used the power they have paid for several months previously.

But a Smart Grid gives consumers the potential to save both energy and money. For instance, you can adjust your consumption so some of it happens when electricity is cheaper. The goal is to be able to see when the price is at its lowest.

"Then you'll notice a difference immediately," said Fosso, who says he thinks this feature will make it easier to save, too.

If electricity is much cheaper at 10 pm, maybe you'll time your car charging for then instead. Or maybe you'll wait a few hours to turn on the washing machine.

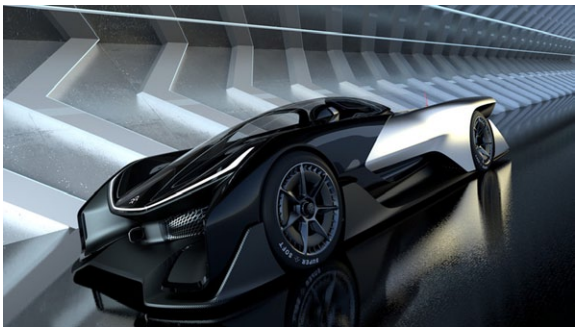
Developing a Smart Grid is a task with many variables. In the future, private households will produce more of their own electricity, which complicates the picture further. Then it will be all the more important for us to use the power grid more efficiently.

There is not much you need to do to reduce consumption. Preliminary experiments show that Smart Grid helps people to save around 10 per cent on energy costs, and peaks loads are reduced by around 15 per cent.

"One kWh saved is as good as one kWh produced. We need to bring the end users on board," said Fosso.

Faraday Future to compete on Tesla's EV market

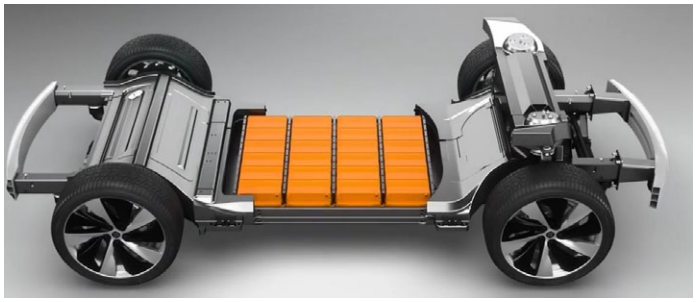
By Paul Buckley



Another new rival to Tesla Motors Inc. in the high performance electric vehicle sector has entered the fray.

Faraday Future Inc. revealed the company's 'concept' electric car at CES 2016 in Las Vega, USA. The four-motor sports car features a modular battery-pack design enabling the vehicle to accelerate from 0-60 mph in under three seconds and achieve a top speed of more than 200 mph.

Backed by Chinese financing the Faraday Future electric car's powertrain features a Variable Platform Architecture (VPA) with a new battery structure that is centrally placed for integrity and arranged into modular 'strings'. Adding or removing the strings changes the overall battery capacity and allows Faraday to develop new wheelbases and crumple zones, which are optimized in each specific zone for safety.



An intelligent, modular approach builds on a flexible battery layout and multiple powertrain configurations offer the potential to deliver a diverse range of vehicles to market faster and more efficiently than previously thought possible.

The Faraday electric vehicle will be designed to offer autonomous driving capabilities from the start, and Faraday also is exploring shared ownership or pay-per-use ownership models. Last month Faraday Future announced plans to launch a state-of-the-art automotive production plant in the near future north of Las Vegas in the USA.

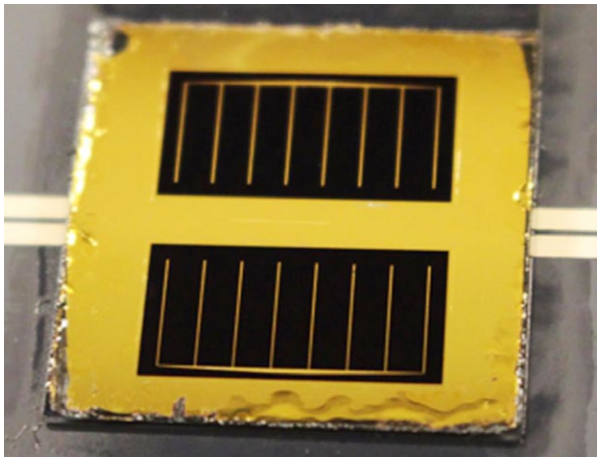
Faraday Future is preparing to invest $1 billion into the first phase of the manufacturing facility which aims to create 4,500 new jobs.

Dual-junction solar cell claims efficiency record

By Paul Buckley

Scientists at the Swiss Center for Electronics and Microtechnology (CSEM) and the USA's Energy Department's National Renewable Energy Laboratory (NREL) claim to have jointly set a world record for converting non-concentrated sunlight into electricity using a dual-junction III-V/Si solar cell.

The newly certified record conversion efficiency of 29.8 percent was set using a top cell made of gallium indium phosphide developed by NREL, and a bottom cell made of crystalline silicon developed by CSEM using silicon heterojunction technology. The two cells were made separately and then stacked by NREL.



"It is a record within this mechanically stacked category," said David Young, a senior researcher at NREL. "The performance of the dual-junction device exceeded the theoretical limit of 29.4 percent for crystalline silicon solar cells."

Young is co-author of a paper entitled 'Realization of GaInP/Si dual-junction solar cells with 29.8 percent one-sun efficiency', which details the steps taken to break the previous record. His co-authors from NREL are Stephanie Essig, Myles Steiner, John Geisz, Scott Ward, Tom Moriarty, Vincenzo LaSalvia, and Pauls Stradins. The paper has been submitted for publication in the IEEE Journal of Photovoltaics.

Essig attracted interest from CSEM when she presented a paper, "Progress Towards a 30 percent Efficient GaInP/Si Tandem Solar Cell," to the 5th International Conference on Silicon Photovoltaics, in Germany in March.

"We believe that the silicon heterojunction technology is today the most efficient silicon technology for application in tandem solar cells" said Christophe Ballif, head of PV activities at CSEM.

"CSEM partnered with the NREL scientists with the objective to demonstrate that 30 percent efficient tandem cells can be realized using silicon heterojunction bottom cells, thanks to the combination with high performance top cells such as those developed by NREL," said Matthieu Despeisse, the manager of crystalline silicon activities at CSEM.

A new design for the dual-junction solar cell and the contributions from CSEM were key to setting the record. The first collaboration results indicate that even greater efficiency can be achieved by the combination of NREL and CSEM cells.

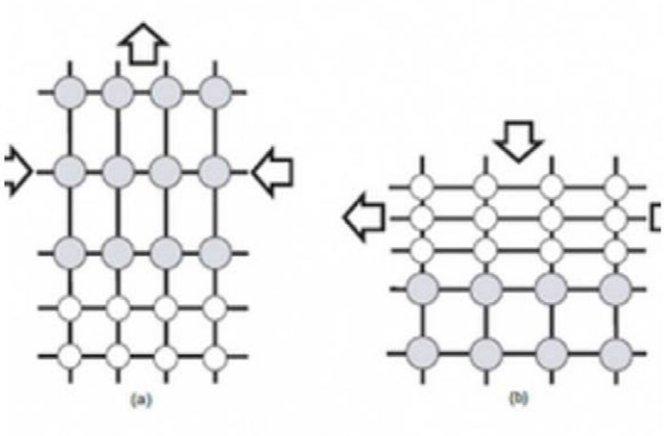
Leti strains to improve FDSOI

By Peter Clarke

French research institute CEA-Leti has reported on two techniques to put local strain in the silicon channel of a fully-depleted silicon-on-insulator (FDSOI) manufacturing process.

STMicroelectronics and Globalfoundries are championing the FDSOI process as a means to achieve world-class energy efficiency in leading edge integrated circuits without the complexity and expense of FinFET manufacturing.

Strain on the crystal lattice is used routinely to increase mobility in conventional planar CMOS and in FinFET CMOS. Leti (Grenoble, France) is now proposing its use on next-generation FDSOI circuits to realise the same benefits; higher performance at the same or lower power consumption.



Two techniques are required because p-channel FETs in FDSOI require compressive strain of silicon-germanium channel material while a tensile strain is required to improve the silicon n-channel FET. The two techniques Leti has developed can induce local stress as high as 1.6GPa in the channel.

The first technique uses the transfer of strain from a relaxed SiGe on top of the SOI film. This has been used to boost short-channel electron mobility by more than 20 percent.

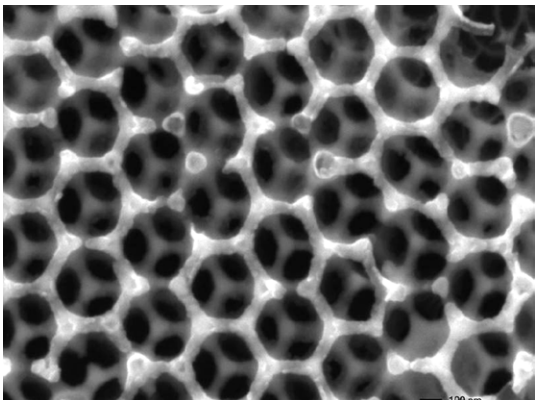
The second technique relies on creep in the buried oxide under high temperature annealing to insert tensile strain in the overlying silicon. BOX-creep can also be used to introduce compressive strain, Leti said.

Such strained channels enable an increase in the on-state current of CMOS transistors and more performance at same power or a reduction in power consumption for a given performance. While stain was not necessary for 28nm FDSOI it is beyond the 22/20nm node, Leti said.

Nanostructured germanium for custom photovoltaics

By Paul Buckley

Researchers at the Technical University of Munich (TUM) and the Ludwig Maximillians University of Munich (LMU) have discovered a procedure using nanostructured germanium to produce thin robust and porous semiconductor layers for portable photovoltaics and battery electrodes.



The material is ideal for use in small, light-weight, flexible solar cells or electrodes that improve the performance of rechargeable batteries.

By integrating suitable organic polymers into the pores of the material, the scientists can custom tailor the electrical properties of the ensuing hybrid material. The design not only saves space, it also creates large interface surfaces that improve overall effectiveness.

"You can imagine our raw material as a porous scaffold with a structure akin to a honeycomb. The walls comprise inorganic, semiconducting germanium, which can produce and store electric charges. Since the honeycomb walls are extremely thin, charges can flow along short paths," explained Professor Thomas Fässler, chair of Inorganic Chemistry with a Focus on Novel Materials at TU Munich.

To transform brittle, hard germanium into a flexible and porous layer the researchers had to apply a few tricks. Traditionally, etching processes are used to structure the surface of germanium. However, the top-down approach is difficult to control on an atomic level. The new procedure solves the problem.

Together with his team, Fässler established a synthesis methodology to fabricate the desired structures very precisely and reproducibly. The raw material is germanium with atoms arranged in clusters of nine. Since these clusters are electrically charged, they repel each other as long as they are dissolved. Netting only takes place when the solvent is evaporated.

Netting can be easily achieved by applying heat of 500°C or it can be chemically induced, by adding germanium chloride, for example. By using other chlorides like phosphorous chloride the germanium structures can be easily doped. This allows the researchers to directly adjust the properties of the resulting nanomaterials in a targeted manner.

To give the germanium clusters the desired porous structure, the LMU researcher Dr. Dina Fattakhova-Rohlfing has developed a methodology to enable nanostructuring: tiny polymer beads form three-dimensional templates in an initial step.

In the next step, the germanium-cluster solution fills the gaps between the beads. As soon as stable germanium networks have formed on the surface of the tiny beads, the templates are removed by applying heat. What remains is the highly porous nanofilm.

The deployed polymer beads have a diameter of 50 to 200 nanometers and form an opal structure. The germanium scaffold that emerges on the surface acts as a negative mold – an inverse opal structure is formed which is why the nanolayers shimmer like an opal.

"The porous germanium alone has unique optical and electrical properties that many energy relevant applications can profit from," said LMU researcher Dr. Dina Fattakhova-Rohlfing, who, in collaboration with Fässler, developed the material. "Beyond that, we can fill the pores with a wide variety of functional materials, thereby creating a broad range of novel hybrid materials."

"When combined with polymers, porous germanium structures are suitable for the development of a new generation of stable, extremely light-weight and flexible solar cells that can charge mobile phones, cameras and laptops while on the road," explained the physicist Peter Müller-Buschbaum, professor of functional materials at TU Munich.

Flexible Bluetooth LE beacon sticker operates on photovoltaics

By Julien Happich

Fujitsu has unveiled a battery-less flexible Bluetooth LE-enabled geolocation beacon, measuring 108x26mm and only 3mm thick. The ready-to-stick beacon features a flexible photovoltaic panel that can generate power from sunlight, fluorescent light, and LED light.

Fujitsu claims the prototype beacon has obtained the world's first ucode tag certification for a beacon from the TRON Forum. It can be easily mass produced and is capable of transmitting a globally unique ID for more reliable location information services. Location codes are sent inside packets. Bluetooth-enabled devices receiving the code send enquiries to a server that manages the location codes thus allowing them to receive locational information. Thanks to this certification, the beacons can be linked with all types of map data that form the foundation for delivering services.

The beacon was produced printing a circuit wiring pattern (with a conductive paste) to which electric components were mounted and connected with conductive adhesive. The paste and adhesive materials were selected to enable mass-production with existing production facilities.

Some application scenarios for these low-cost battery-less Bluetooth LE beacons include location information services such as guidance support for the visually impaired within stations or around town, or efficient seat management for stadiums.

The conformable nature of the tags makes them suitable to be affixed to clothes and shoes, extending use cases to user-centric applications.

Visual, haptic, smart: innovative HMI tech at CES

By Christoph Hammerschmidt

The interaction between driver and vehicle, almost unchanged over decades, is arriving in the digital age. At the Consumer Electronics Show (CES) in Las Vegas, novel approaches give ideas how digitisation affects the way drivers will control their vehicles in the future.

Perhaps one of the most striking presentations at the fair can be seen at the BMW booth: the Bavarian carmaker shows a study of a future car based on its i8 sports vehicle. The i8 Concept Spyder is equipped with an 21 inch wide, 4.3 inch high display panel that visualises anything related to connectivity, mails, telephony (even video telephony, as long as the vehicle is not driving), or internet services as well as real-time navigation. While this display is located at the passenger side, the driver has full visibility of the relevant representations.

The cockpit of BMW's i8Concept Spyder is dominated by a 21" x 4" display.

This large display screen is complemented by a smaller screen above the steering column that displays all the usual car-related information, plus a head-up display that informs the driver about road, traffic (thanks to V2X communications even cars beyond the direct visibility are depicted), obstacles, road signs and the like. To enter a command, the driver or passenger uses BMWs AirTouch gesture recognition feature that enables users to interact with the display without the need to touch them: sensors detect hand movements in the space between the centre console and the inside mirror and translate them into control activities, enabling him to select menu items, accept phone calls or set the volume of the infotainment system.

While a gesture recognition feature is already available in BMWs current 7 high-end series, AirTouch is more advanced, the carmaker says.

Competitor Audi demonstrates the HMI concept for future vehicle generations by means of an interior model. The carmaker has further developed its known MMI user interface in that it is now centring around a large (albeit smaller than BMWs) AMOLED display with haptic feedback. The system detects gestures familiar from the interaction with smartphones and adapts them to the automotive environment.

Audi emphasises the in-car connectivity: the infotainment system, built around the company's next-gen modular infotainment kit MIB2+, supports smartphone and smartwatch integration as well as the fourth generation of Apple TV. In addition, the carmaker announced to introduce first Car-to-X services within the year 2016. For Europe, Audi plans to introduce traffic sign information and hazard information; in the US, the company will roll out a traffic light service that connects the car through mobile connections to the central computers that control the traffic lights at city level.

Gesture recognition, AMOLED display and Car2X services: Audi`s recipe for the automobilistic future

Not as spectacular as Audi's and BMW's concept studies, but technologically sound: ZF shows the building blocks for future HMIs

Deeper looks into the underlying technology provides automotive supplier ZF Friedrichshafen, after the takeover of its US competitor TRW one of the first-league players in automotive electronics. In its Concept Cockpit, ZF shows three building blocks for future automotive Human Machine Interfaces.

ZFs multi-functional steering wheel simplifies the takeover phase between automated and manual driving. Thanks to an integrated hands-on/hands-off detection, the vehicle knows if the driver is really ready to take over command. In parallel, a LED line provides something like an optical countdown to the driver, displaying the time left until he must take over. The push-to-drive button at the wheel allows him to terminate automated driving and switch to manual immediately.

The Swipetronic panel provides a digital shift-by-wire alternative to automated transmissions. It is based on a touch display at the place where normally the mechanic gear lever is located. Using the principle of electrostatic charging, it enables users to feel and palpate the virtual switches on the screen as if they were conventional electromechanical switches. Thus, drivers do not need to look down at the screen any longer to select a function but instead can continue to focus on the traffic, a contribution to reduce drivers distraction. The Swipetronic panel corresponds with an electronic circuit that enables customers (carmakers) to customize all functions including transmission ratio by software. While shown as a user interface for a transmission, the Swipetronic can be used to control just about any function in the car cockpit, ZF explains.

Another new development is dedicated to the detection of drivers' attention (or the lack hereof). The company utilises camera-based facial recognition to determine if the driver tends to become sleepy or inattentive. Like a similar system shown by Harman at the CES, the ZF system also detects the viewing direction; algorithms then process the information and assess the drivers' attention, enabling designers of driver assistance systems to develop systems that support the driver with matching actions.

Startup raises funds for battery-less IoT

By Peter Clarke

PsiKick Inc. (Charlottesville, Virginia), a semiconductor startup formed to work on sub-threshold voltage operation wireless circuits, has raised $16.5 million in Series B financing led by Osage University Partners and joined by existing investors.

The company was founded by professors at University of Virginia and the University of Michigan in 2012 and raised a Series A round of finance in 2014 reported to be worth $5.25 million. This brings total funding raised by the company to more than $22 million.

The startup has designed a proof-of-concept wireless sensor node system-chip using conventional EDA tools and a 130nm mixed-signal CMOS that operates with sub-threshold voltages and opening up the prospect of self-powering Internet of Things (IoT) systems. The company has claimed that its proof-of-concept chip design would consume between 100 and 1000 times less than any comparable chip.

The latest tranche of funding will be used for expansion of engineering and developing battery-less systems based on the sub-threshold technology, the company said.

"Prior to Series B, PsiKick created a platform of fundamental technologies for wireless devices that are entirely self-powered," said Brendan Richardson, CEO of PsiKick, in a statement. "Those building blocks include the world's most efficient wireless connectivity, robust node computation and energy harvesting to enable a highly scalable batteryless IoT," he added.

Marc Singer, managing partner of Osage University Partners, is set to join PsiKick's board of directors as part of the Series B financing deal.

As part of its proof of concept progress PsiKick is working on systems that can scavenge energy from multiple sources including indoor light, RF rectification, thermal gradient and piezo-electric vibration. One such system is a battery-less electrocardiogram (EKG) sensor that supports a 1Mbit per second data rate over 10 meters distance.

Other companies working on sub- and near-threshold operation of ICs include fabless startup Ambiq Micro Inc. (Austin, Texas) and ARM Holdings plc (Cambridge, England). Ambiq has launched the Apollo line of Cortex-M4F based microcontrollers claiming they offer a 10x reduction compared with other microcontrollers and ARM has been working in R&D on a processor core optimized for operation close to the threshold voltage of CMOS transistors and at clock frequencies of the order of tens of kilohertz.

Leading foundry TSMC has developed a series of processes characterized down to near threshold voltages, such as 0.6V. The ULP family for ultra-low power are processes, introduced at the 55, 45, 28nm planar CMOS and the 16nm FinFET nodes.

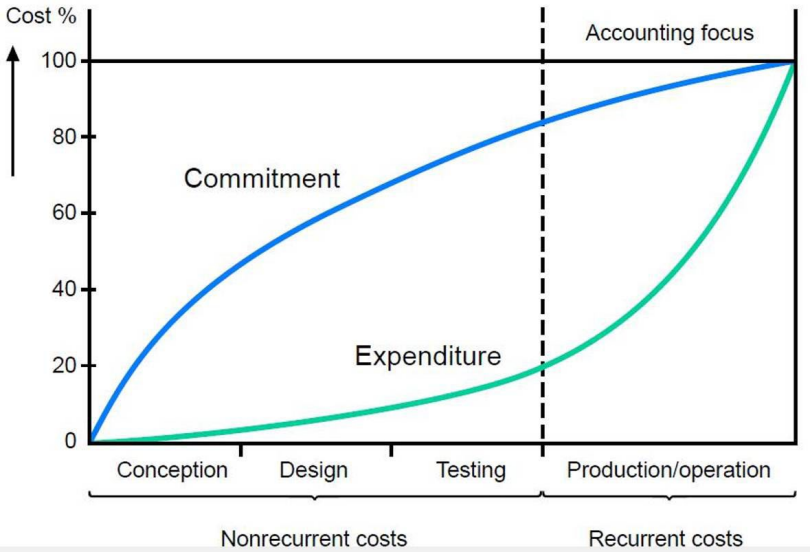
Why test?

By Peter van den Eijnden

Design for Manufacturing (DfM) rules and highly automated assembly equipment minimize the number of assembly errors on your printed circuit board assemblies (PCBAs). To deliver fault free, high quality PCBAs they must be tested to detect and remove any remaining assembly errors. Detection of such errors as early as possible, ie at board level before system level assembly, is crucial to save costs.

The amount of money that will be spent on testing in manufacturing (the recurring costs) and in field service is determined by the testability of the design and hence is committed during the design phase of the product. The relationship is shown in the figure below.

If during the design phase no attention is paid to testing at all, then it should come as no surprise that testing the board in manufacturing can be very expensive. Maybe certain nodes cannot be controlled independently by the tester (eg a reset pin directly tied to Vcc or ground) or the possibility to find the cause of a fault - the fault diagnosis - may get very complex.



Miniaturization and increasing device complexity

Smaller device packages and increasing device complexity limit the test coverage and diagnostic capabilities of traditional test methods like in-circuit test (ICT), flying probe test (FPT) and functional test (FCT). JTAG test and in-system programming applications use the resources built into the chips on your boards and are complimentary to the traditional test methods. Combining JTAG with traditional test methods results in higher test coverage for all types of boards.

JTAG boundary-scan added to an ICT/FPT specifically helps to restore test access. JTAG boundary-scan added to a functional test systems helps to detect and diagnose manufacturing defects more easily. Also it can help to more easily create specific starting states for the functional test on a board, or to inspect signal states at any point during the functional test.

DFT rules

Using the latest test technologies and applying Design for Test (DfT) rules results in boards that are better testable and helps to minimize the costs of testing in production.

The JTAG interface on many of today's devices provides an excellent opportunity to limit the recurring test costs of a printed circuit board.

Through this interface test and in-system programming on a board is possible using the resources built into the chips on a board. By taking a few simple Design for Test (DFT) rules into account different JTAG test and programming applications can easily be created, and can be used efficiently in manufacturing as well as field service. A complete overview of Design for Test rules at board and system level can be found in JTAG Technologies' DFT booklets. Both are available for free through our website: www.jtag.com.

Peter van den Eijnden is the managing director of JTAG Technologies - www.jtag.nl

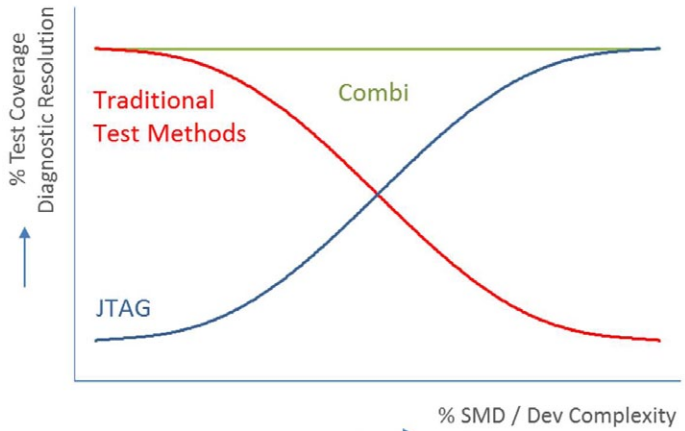
Check testability and fault coverage

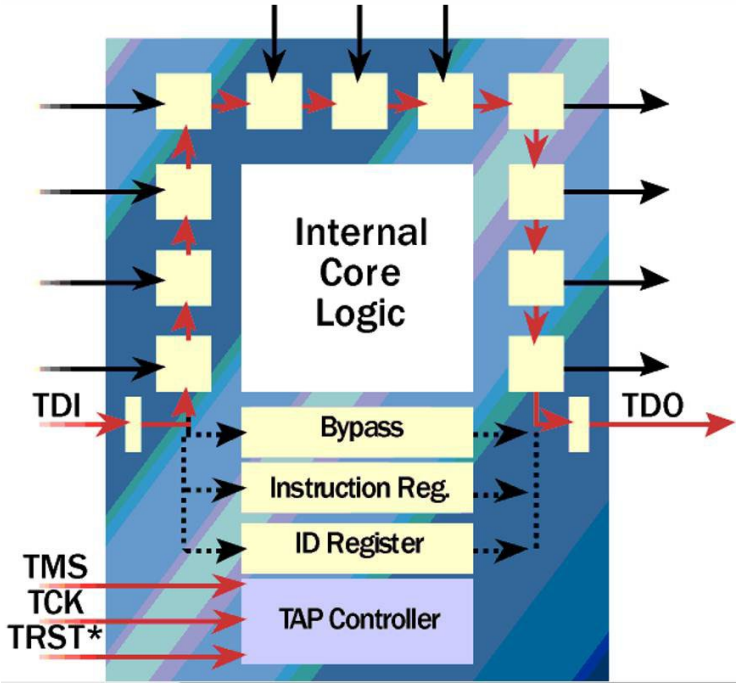
When JTAG testing is used you can calculate the testability of your design. A product like JTAG ProVision includes integrated testability and fault coverage analysis with details of the net and pin-level testability. If your testability goals are not met, you can correct your design as it progresses, right on your schematic and layout drawings.

Comparing the total coverage of the created applications against the calculated testability of the board quickly reveals if additional tests need to be developed. Closely watching the testability of your design and fault coverage of your tests not only limits the test costs, but also helps to get products to market faster with higher quality levels.

JTAG for testing and in-system programming for prototypes and small production series

JTAG test and in-system programming use the resources (boundary-scan registers, debug registers, etc.) built into the chips on your boards. These embedded resources can be accessed with a simple JTAG controller that interfaces your PC with the JTAG interface on your board. For higher demands advanced, high performance JTAG controllers are available.





The applications, debugging, testing, in-system programming of programmable logic (FPGAs and (c)PlDs) or flash memories, etc. are determined by the software being used. For basic testing buzzing-out connections interactively and interactive verification of a cluster (ie a non-boundary scan device surrounded by boundary-scan devices) may already be sufficient. More functionality and automation, eg automatically generate various JTAG boundary-scan applications, run a sequence of test and in-system programing actions, etc. can simply be added by further software modules.

A simple controller plus some interactive test capabilities in addition to your normal functional test set-up may be sufficient for debugging and testing prototypes as well as small production series. The JTAG controller plus test and in-system programming software can be used stand-alone, or be integrated with your functional test set-up.: “JTAG Technologies inside”.

You can thus scale your JTAG test and in-system programming solution from a simple controller with some basic test software all the way to a fully equipped system with automatic application generators and advanced sequencing capabilities. This makes JTAG a cost-effective approach not only for higher volume production, but also for prototype testing and small volume production.

Even if only one device on the printed circuit board assembly (PCBA) has boundary-scan JTAG testing can already be used. The more JTAG access is available on a board the higher the fault coverage via JTAG. The amount of JTAG access on a board not only depends on the number of boundary-scan devices that is present, but also which device types have boundary-scan. If in a CPU-centric or FPGA-centric design only the CPU or the FPGA has boundary-scan and/or a JTAG debug register the fault coverage via JTAG can already be very high.

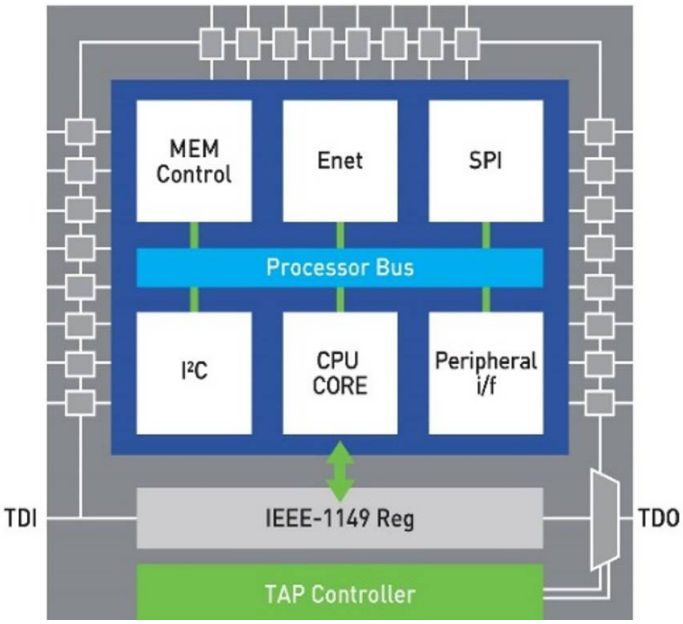
Covering analog and digital

Boards contain a mix of analog and digital circuitry. JTAG boundary-scan is mostly limited to digital signals (although an analog boundary-scan standard does exist). When JTAG is combined with functional testing the analog signals are often handled by the analog instruments used for the functional tests. When JTAG is combined with ICT and FPT systems, often used in higher volume production, similarly the analog circuitry is handled by the ICT or FPT. To handle the analog circuitry of a board in a stand-alone system Mixed-Signal I/O capabilities are available with JTAG Technologies’ boundary-scan systems (JTAG controllers, I/O modules and software).

Background on JTAG boundary-scan

With boundary-scan a shift register is added in silicon along the pins (the boundary) of the chip. With each (digital) pin of the chip one or more cells of this shift register are associated. Through these cells one can now control and / or observe a device pin independent of the functionality (core logic) of the chip.

The connection between the pins of two, or more boundary-scan chips can easily be verified. All it takes is to drive a 0/1 on an output pin via its bit in the bscan reg and then observe the value seen by the connected input pin(s) via their bits in the bscan reg’s of the chips.



This forms the basis of boundary-scan.

In this way the connections between bscan devices can easily be verified, even if other non-bscan devices are in between. A very simple example of such device would be a series resistor.

When bscan devices are connected to the address, data and control pins of a flash memory then this memory can be written to and read from via the bscan registers of these devices. In this way in-system programming of flash memories via JTAG is possible.

Microprocessors often contain special JTAG accessible debug logic for software debugging purposes. This logic may be in addition to a boundary-scan register in the chip. Sometimes, however, a boundary-scan register is not present in those chips. Through the debug logic one has full JTAG control over the CPU core and its busses and everything connected to it. This debug logic can now be used for test and in-system programming purposes (emulative test and programming).

JTAG Technologies’ CoreCommanders interface directly with the debug logic of a microprocessor and provide full control over a processor core. CoreCommanders are specific for a processor core, a processor type, or processor family. The functions of a CoreCommander – its API – are independent of the type of processor core.

Avoiding the costs of inadequate ECAD/MCAD & design data management

By Robert Huxel

It is a truism that only a part of a design engineer's time, in the course of his or her daily tasks, is spent actually designing. Sometimes that proportion can be frustratingly small; of the time spent carrying out ancillary functions, managing information can account for a large part. Automation – as with all applications of information technology – can make a big difference, but only when the systems applied are properly focussed on the task in hand.

Printed board design can be viewed as the pivotal design function. Looked at in one direction, it both defines and is constrained by the overall format of the final product: there is an exchange of information with the mechanical world (ECAD to MCAD in terms of design systems) that relates to the external dimensions of the product, and to how the electronic assemblies are packaged within the outer casing.

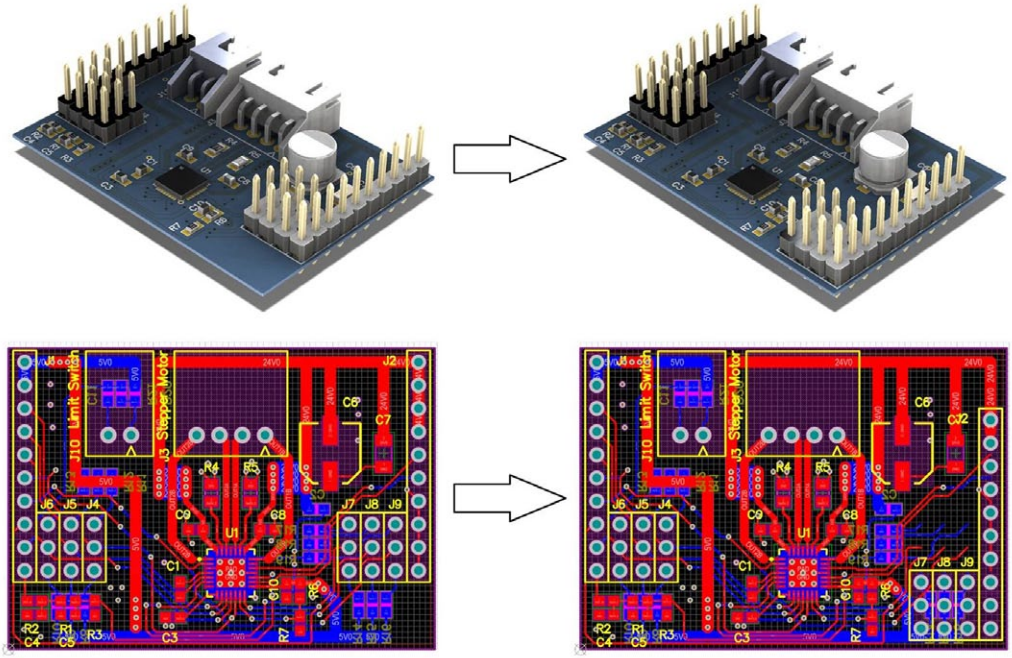
From another perspective, the PCB is where all of the work that goes into circuit design is focussed; and to that can be added everything that goes into component selection and procurement; plus all the effort that is invested in verification in the electrical, mechanical and thermal domains.

All of these aspects represent information that has to be sourced, maintained and exchanged between a variety of systems. Viewed from that high level, it is clearly desirable that the various stages of, and tools used in, the design process should access common data formats and exchange information in as seamless a fashion as possible. The reality that many engineers have been used to working with, however, falls some way short of that ideal.

The interface between mechanical and electrical (PCB) design environments is a well-known case in point. The PCB, in all three dimensions, must fit in some form of enclosure. The available space may be pre-allocated, or it may be designed around the PCB. In either case, development demands an exchange – in practice, repeated exchanges or iterations – between mechanical and electrical design spaces.

Over time, a variety of off-the-shelf and "home-built" systems have evolved to facilitate this exchange; where files are passed back and forth between ECAD and MCAD, two file formats have been in common use. IDF (Intermediate File Format) is long established but falls short of passing comprehensive geometry. It is not a full 3D representation, rather a layout or footprint plus height of individual components (from component models, of which more later).

STEP (Standard for The Exchange of Product model data) takes things forward a stage with a true 3D representation of design data and can be used for PCBs, components, mechanical assemblies/housings, and any other design files which may be collaborated on by multiple designers using different programs. But this still involves exporting and importing files between software packages, with all that implies for version control and the opportunities for error. There are benefits, and limitations, associated with using STEP for bi-directional transfer between programs.



True ECAD/MCAD collaboration gives designers visibility into incremental design changes. Both designers can see component placement changes simultaneously and make any necessary alterations in response.

Native 3D PCB editing tools running within ECAD software for mechanical design, or at least alignment, placement, and export of 3D mechanical models, allow much of the work to be done in a single software package. Altium Designer, for instance, includes capabilities for aligning 3D component models to footprints, modelling and clearance checking for housings/enclosures, and if necessary, standard exports of complex PCB features for MCAD interfacing. More recently, Altium created a new PCB tool that comprehensively integrates PCB data with full 3D CAD in SolidWorks.

The true costs of not having a coherent link between ECAD and MCAD can be considerable. They can manifest themselves as missed schedules and extended time-to market; inefficient

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use of skilled staff, perhaps leading to higher headcount than would otherwise be necessary; and designs taken to market in a less elegant form (due to restricted opportunity for design exploration) leading to reduced sales. Added to which are the immediate development-budget impacts of repeated prototype revisions.

Any significant error can result in an unwanted prototype spin. Getting a conflict-free outcome on the first iteration is, in reality, only the first step. The design process will typically require a number of revisions and changes – even without adding any that arise from file transfer errors. As with any development, the cost of a change order rises sharply as the design proceeds. On average, Engineering Change Orders (ECOs) cost about €1,800 to implement during development, rising to almost €10,000 once a design has been released to manufacturing.

There can be more subtle costs resulting from not having an automated data exchange, or not having confidence in the passing of accurate parameters. Tolerances and clearance allowances can be increased "just to be sure", resulting in designs that are larger than they need be, using more materials and costing more in their BoM.

In an era of ever-more compact and portable products, this is increasingly unacceptable. Or, designers can resort to traditional methods of ensuring fit and clearances, such as paper/card space models ("paper dolls"). Aside from the wasted resource of having skilled circuit and board designers spending their time making cardboard cut-outs, these cannot accurately represent aspects such as bend radii of rigid/flex assemblies – which can be completely modelled in current Altium Designer releases.

More recently, technology has offered the alternative of a 3D printed space model to evaluate form-and-fit. These can be valuable as an aid to giving a real-world impression of how the end product will look and feel; but compared to an integrated ECAD/MCAD environment, they are a very limited verification vehicle to confirm fit and clearance data.

A typical conventional design flow will start with a draft layout that may be set by mechanical ("it has to fit in this space") or electrical constraints ("the PCB layout logically looks like this, design the enclosure around it"). In either case, if the first-pass PCB fits the draft case, with all components falling within their expected envelopes and no unexpected conflicts, then that layout can become "untouchable".

Any major revisions are simply too painful. With a seamless design environment, both electrical and mechanical designers gain the ability to explore alternative layouts and shapes in the virtual environment, without incurring the costs of a major design re-spin for every variation.

A PCB layout must be populated with components, and a comprehensive and accurate component library is a further key aspect of the integrated design environment. For many years one of the impediments to operating an integrated PCB and 3D design environment was the limited availability of component data. If accurate dimension data was unavailable for even a relatively small fraction of the overall BoM, the effort of setting

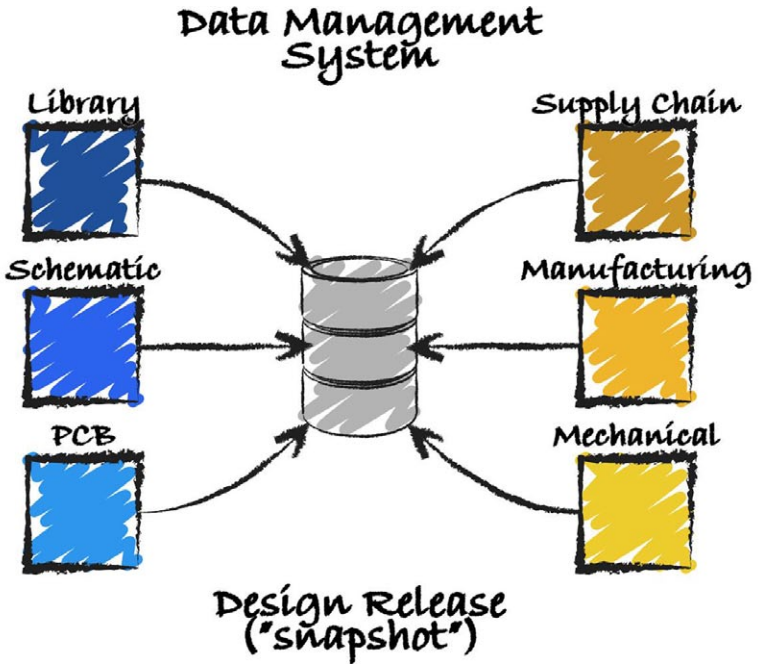
up a CAD-based flow was largely negated. Today's situation is much improved with component manufacturers and their distributors making dimensions and parameters routinely available in common formats.

As with the ECAD/MCAD interface, there are great benefits to having a "joined-up" design environment with full access to all aspects of component data. The circuit designer first comes to component selection from the electrical/electronic performance aspect, but that is only a part of the complete description of a component that resides in the full database.

Other attributes include a physical model, with complete geometry (and rendered visualisation); symbol; PCB footprint; and visibility into the e-commerce supply chain for real-time availability and pricing information. The data sets will also include a part's status; has it been approved, or superseded?

Is it "recommended for new designs" – or has it been tagged as end-of-life? Is it preferred, are there similar parts that meet the requirements?

Have any issues arisen with use of the part in the past? If it must be added to the library, what is the lead time to do so?



A design release encompasses all information from the design side and other relevant domains for bringing a product to market.

The power of having that data tightly linked to the design environment hardly needs stating. Less obvious, perhaps, are the potential costs of inefficient management of ECAD libraries. Inefficient processes can add to administrative overhead, with increased operational cost through redundant or non-centralised infrastructure, and can lead to duplication of effort in – for example – sourcing and qualifying similar parts to those already listed, instead of exploiting common librarian and preferred electronic component lists. This in turn can push up inventory cost, with redundant parts being stocked and, eventually, obsoleted and written-off.

Component data of less-than-ideal quality also has costs. Incomplete information or insufficient part qualification processes can leave room for ambiguity and may cause costly rework of the product when design verification reveals shortcomings, delaying volume production and shipping. Worse, the issues may go undetected until after product introduction, with quality, reliability or compliance problems with the end product.

The integrated library and ECAD/MCAD design environment must therefore not only provide seamless support to the design processes. Of necessity, it must also have a comprehensive set of tools to manage the data held within it – in other words, not only a library, but all the tools needed by the librarian. This includes comprehensive access control; who has the authority to create, modify, delete parts, as opposed the designer's need to access, import into a project and, where necessary, add commentary.

A number of options exist to implement this function; it can be – and frequently has been – provided by custom-built, internally-developed (internal to the user's organisation) solutions. These largely stand apart from the CAD/EDA environment and are difficult to integrate closely, lacking the ability to track and conform to evolving industry standards. Alternative solutions include those based on a product life-cycle management platform, but these, too, can lack the ideal level of integration.

Key performance metrics related to an integrated library solution can be stated as:

- Increased engineering efficiency
- Shortened design cycles with fewer library- and component-related design spins
- Improved product quality through approved vendors and parts, reduced inventory cost and new part introductions
- Improved overall library quality leading to fewer issues downstream
- Reduction of infrastructure cost and overhead.

To meet these needs, Altium has conceived and evolved its Altium Vault. With rigorous control of access and authentication of users, the Vault provides component data repositories with all of the attributes needed by the ECAD/MCAD flow. It embodies complete revision control and lifecycle management, both for objects acquired (i.e. components) or assemblies manufactured. The organisation using it has, effectively, its own part catalogue from which to select, built around its own priorities and with visibility into the supply chain.

Parts lists and bills-of-materials are checked in real time for issues – either historical or anticipated – with any devices listed, and will be held from release until all such issues are resolved. The Vault gathers all expected and required information in one system, with no data redundancy; it supports fast component searches with integrated supply chain information. Geographically distributed users can have worldwide access via Intranet to a single database; and the engineering function gains data consistency from the design process to board assembly.

Continuing the momentum of formal verification

By Chi-Ping Hsu

Verification solution providers seem to agree that it takes a family of engine technologies to efficiently cope with verification complexity. One of the critical members of that family is formal technology. Long known for the completeness and finality of its analysis, where applicable, formal has nonetheless been difficult to harness. There has been a shortage of expert users who understand the strengths and weaknesses of the underlying engines, along with the ultimate task at hand—the verification of a production SoC.

However, encapsulation of formal technology use cases into "apps," along with methodologies that contribute high verification value without requiring formal proofs to complete, have opened the door for "every man's" formal technology. In 2015, formal verification is already a mission-critical technology for customers. In 2016, we can expect formal engines to continue growing in popularity with verification teams.

Verification has always involved a family of technologies that need to be used together: simulation, emulation, FPGA prototyping, formal approaches, software-based verification.

But historically, formal verification has been a difficult technique to adopt, since it has largely consisted of the formal engines requiring a lot of user expertise that hasn't been broadly available. The reputation that it took a PhD in formal verification to be able to use the tool was not that far-fetched.

However, formal tools have been democratized by two relatively recent developments: first, the emergence of apps that handle specific use cases that are very accessible to any verification engineer; and second, the emergence of methodologies, such as formal bug-hunting flows and the use of "bounded proofs," which do not require formal proofs to actually complete in order to add substantial value to today's verification flows.

As a general rule, simulation is good at verifying the normal use cases of a block or an SoC, but formal finds the corner cases that nobody even thinks about. The apps make formal easy to use for straightforward cases by automating both the creation and proving of properties, also known as assertions, to fully verify these cases. Meanwhile, for more involved cases, bug-hunting flows and automated analysis of the verification achieved with incomplete (bounded) proofs have made it much easier for non-experts to derive huge verification value from incomplete exploration of assertions. Both of these recent developments have helped drive the use of formal verification forward.

Most formal verification companies have switched to apps to get away from the "must have a PhD" stigma. Apps can make it easier to do the easy things and also provide functionality for more difficult tasks. For example, there are "boring" things like making sure that the microprocessor communicates correctly with the peripherals at the correct register addresses. This task requires a lot of simulation, but formal approaches can handle this fairly easily.

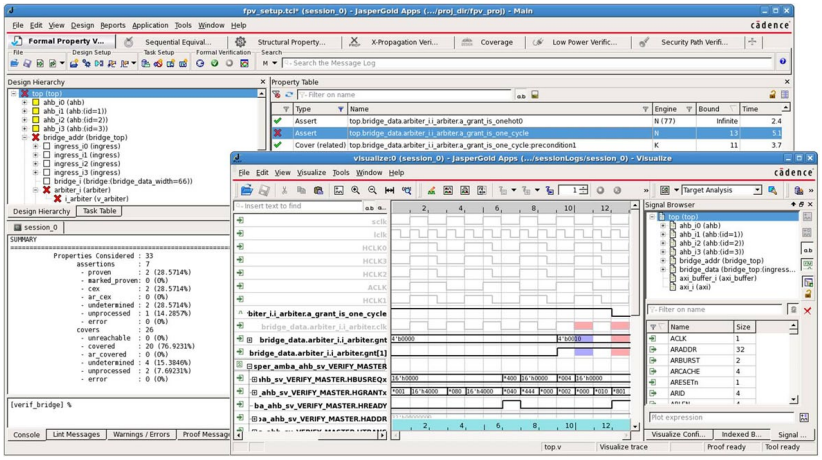
There are now apps available for an array of targeted use cases. As an example, consider sequential equivalence checking. Power reduction has meant that netlists are not updated with a full preservation of register equivalence. They may be negated or even delayed if they do not need to be updated. The basic idea is that if a change to a register will never be noticed, then you can save power by not updating it. As a result, it will have the wrong value, which throws off traditional logical equivalence checking (LEC). A sequential equivalence checking app can input two RTL files and quickly verify their sequential behavioral equivalence.

There are many other examples of useful formal apps. A security app can check that your keys cannot be leaked, or changed, by code that is not meant to have access to them. That is something that you probably really want to prove, rather than simply rely on a good choice of simulation vectors. A low-power verification app can help you verify low-power designs with multiple power domains, voltage islands, power shutoff, clock shutoff, and all the other techniques used for reducing power.

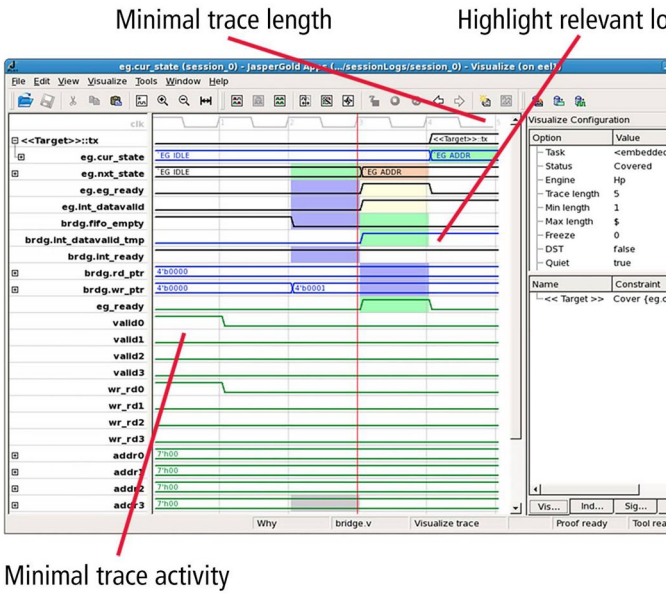
Of course, power is the main driver of SoC design these days, whether it is for mobile chips (in which extending battery life is paramount) or high-performance chips (where power limits how fast the design can be clocked). Very few designs are lucky enough not to require aggressive power management. In fact, it's hard to believe that any major SoC doesn't have power as a major constraint. So verifying the entire power architecture is an important step.

Bug hunting and bounded proofs

As mentioned earlier, formal is great at finding corner cases that the verification engineer doesn't think about. We make great use of this capability in bug hunting. Here, rather than creating a test-bench that attempts to cover all eventualities, the verifica-



Chi-Ping Hsu is senior vice president and chief strategy officer for electronic design automation (EDA) products and technologies at Cadence – www.cadence.com



tion engineer applies some assertions on the design outputs, which are essentially statements about functional behavior that should hold true.

Then the formal engines busily try to find examples where the assertion does not hold true. For each case the tool finds, a short signal trace is created showing the combination of events that would disprove the property. This trace is called a counter-example (CEX). Each CEX the tool finds is a possible bug. The latest formal tools have engines that are dedicated to penetrating the design state space, widely and deeply, seeking out these CEXs, thus removing bugs from designs, without even the intention of completing the formal proof!

In other cases, when all CEXs have been removed, it's important to be able to answer the question, "Is the design fully verified?" If the requisite number of formal proofs have completed, the answer is "yes."

In order to reach this conclusion, the coverage achieved by the set of assertions needs to be analyzed. Again, leading formal tools have this capability. If sufficient assertions have completed, then the verification is absolute, but achieving this happy state on designs of today's complexity can be highly challenging. To address this issue, some formal tools can analyze coverage attained from assertions whose proofs did not complete. These assertions may have been shown to hold true for a certain cycle depth. We call these bounded proofs, and with the right analysis, these can be of great value and effectively extend the value of formal's absolute proof nature to a wider and larger class of designs.

Summary

The big advantage of formal apps is that they do not require deep formal verification expertise. Anyone who can run simulation can use apps to find problems in specific areas that would otherwise require a lot of vectors. Additionally, given just a simple set of assertions about the design's functional behavior, it's easy for any verification engineer to go bug hunting. Of course, expert users can take advantage of the full power of the engines, which have improved immeasurably over the last few years. Even when proofs don't complete, we know definitively what has and has not been verified, using bounded proof analysis. But the big change is in usability. People who are not formal verification experts can accomplish a lot that is easy to do formally and hard to do with simulation. And once you have proved something formally, there is no need to ever prove it again with some other approach. Formal will continue to be mission critical in 2016.

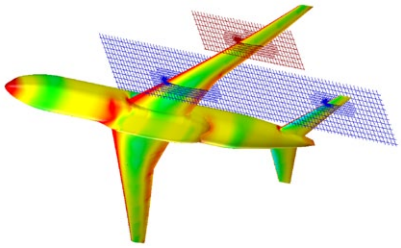
Ultrasoc cores provide 'bare-metal' security

Ultrasoc Technologies Ltd is moving into active functionality by providing support for "bare-metal" security. "Debug is a valuable thing but we realized you can do a lot of other things with the analytical cores we provide," Rupert Baines, the company's CEO, told EE Times Europe. "For example our on-chip debug support is dynamically aware of what cores are in use and what cores are not." While the activities that Ultrasoc could support on-chip are diverse including dynamic voltage and frequency scaling (DVFS) to achieve power savings the first chosen activity is security. The Internet of Things and the connected car in automotive are expected to be the initial applications for the technology. The Ultrasoc support hardware is able to monitor accesses to different regions of memory and raise flags if a process enters a forbidden region, it can monitor software behavior patterns and code sequences. Most security is provided above the level of the operating system, said Baines, but this is complementary "bare-metal security" that is non-intrusive and remains robust even if conventional security measures are compromised, he added. This functionality is provided by the same set of gates that have established benefits for developing an SoC and includes that benefit of supporting multiprocessor and heterogeneous systems. "It's another use case for the same gates, although there will be an incremental license fee and royalty for using the bare-metal security features," Baines added. Ultrasoc's debug support comes as a tool box with up to about 30 different debug functions supported by a number of cores. The typical overhead in terms of gates as a proportion of the total varies between 1 or 2 percent and 7 percent. By adding the security use case it means the Ultrasoc debug support is functionally active after IC deployment as well as in the design phase pre- and post-silicon implementation. Although it functions below and outside of the operating system, the technology also provides a means of communicating with software on the device as part of a holistic security system, if this is necessary. Bare-Metal Security features also provide visibility of the whole system, making it extremely difficult to camouflage or hide an attack. Although originally developed for debug and silicon validation, UltraSoCs IP also enables a broad range of value-added functionality in-service, of which security is just one example. Other applications include in-field monitoring, performance optimization, reducing power utilization and SLA enforcement. UltraSoC's announcement coincides with the inaugural conference of the IoT Security Foundation in London whose aims is to maximize the benefits of the IoT by promoting knowledge and best practice in excellent, appropriate security to those who specify, make and use IoT products and systems.

Ultrasoc Technologies Ltd.
www.ultrasoc.com

Fluid flow/heat transfer CFD package updated

Mentor Graphics has a new release of its FloEFD computational fluid dynamics product that offers improved accuracy and user productivity. Updated features in this new version include improved mesh handling, an enhanced transient solver, a robust EDA interface, and an interface to Abaqus Finite Element Analysis (FEA) software for stress analysis. The package targets engineers and specialists across the automotive, aerospace and electronics markets. The latest version of the FloEFD product offers new capabilities for minimising user time and effort spent on meshing. The FloEFD tool can automatically fill gaps of specified size to quickly make the model watertight, thereby eliminating the time and necessity to adjust the original geometry. An equidistant refinement capability lets users build multilevel uniform meshes around the body or surface of the model with just one click.



Mentor Graphics
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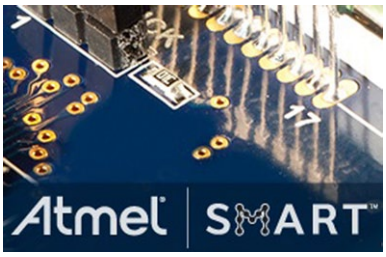
Power insights for ULP projects on Atmel MCUs

Targeting ultra-low-power (ULP) designs for internet of things, wearables and other applications requiring extremely low power, debug tools from Atmel enable developers to identify and eliminate power spikes during development. The high-accuracy debugging tool enables users to visualise the power usage of their product during the development cycle; being able to locate code where power spikes occur is crucial for supporting extremely low power in the overall design. The Power Debugger is Atmel's latest development tool for debugging and programming Atmel | SMART ARM Cortex-M–based MCUs and Atmel AVR MCUs that use JTAG, SWD, PDI, debugWIRE, aWire, TPI or SPI target interfaces. In addition to standard low-level debug functionality, the Power Debugger features two independent current-sensing channels for collecting real-time power measurements during application execution.



Atmel
www.atmel.com

Extended debug support for RL78 in IAR's IDE

Support for the C-STAT static analysis tool, as well as stack usage analysis, is introduced by the latest release of IAR Embedded Workbench for Renesas' RL78 MCUs. This version of IAR Embedded Workbench for Renesas RL78 embedded development tools includes functionality enabling simplified development and increased code quality control for applications based on Renesas low-power RL78 microcontrollers. The add-on C-STAT product for static analysis is now supported. C-STAT features static analysis that can detect defects, bugs, and security vulnerabilities as defined by CERT C/C++ and the Common Weakness Enumeration (CWE), as well as help keeping code compliant to coding standards such as MISRA C:2004, MISRA C++:2008 and MISRA C:2012.

IAR Systems
www.iar.com

Avoiding amplifier output driver saturation

By Jon Munson and Kevin Scott

When taking sensor measurements, the type of sensor excitation used varies greatly; it can be a DC signal, an AC signal, a voltage source, a current source or a pulsed source, to name a few. When using current source excitation or when using a high impedance sensor, the amplifier's bias current is often an important specification, as it can create an undesirable voltage error term as the bias current flows through an external resistance. For this reason, low bias current amplifiers are often required in many of these applications.

This is shown pictorially in Figure 1, where the LTC6268 500MHz femptoamp bias current FET-input amplifier is used to convert photocurrent into a voltage measurement. Ideally the photodiode current (IPD) would equal the feedback current (IFB) and IBIAS would = 0. In actual practice, a zero bias current amplifier is unrealistic. However, the LTC6268's ±3fA typical bias current and ±4pA overtemperature bias current sets the standard for wide bandwidth, low bias current amplifiers.

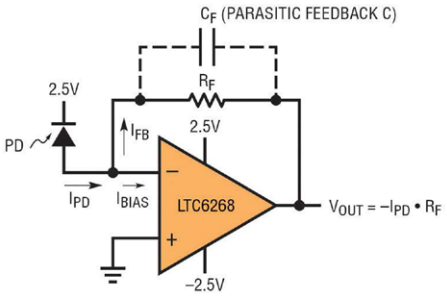


Fig. 1: IBIAS error in photodiode signal conditioning application

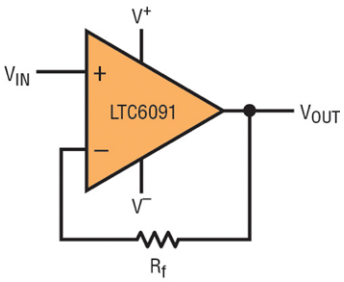


Fig. 2: LTC6091: Saturated output may cause input common mode violation

Output saturation

Sensors that require low bias current amplifiers include photodiodes, accelerometers, chemical sensors, piezoelectric or piezoresistive pressure transducers, and hydrophones. Using a low bias current amplifier with a high impedance sensor can cause problems if the amplifier's input is overdriven, which can lead to an increase in bias current. When this occurs, the amplifier may get "stuck," with the input signal no longer capable of pulling down the output signal to remedy the condition. The LTC6091 buffer circuit in Figure 2 is an example where this can easily occur. The LTC6091 is a dual, 140V precision amplifier with only 50pA bias current (max at 25°C), a rail-to-rail output swing and only 50µV of input offset voltage. Its common mode range is limited to 3V from the power supply rails. To understand what is happening, let's first look at the input stage of the amplifier, as shown in Figure 3.

Amplifier input structure

The input stage consists of +INA and -INA, which are the gates of the amplifier's first stage N-MOSFET differential pair. When the output saturates due to an input overdrive, there needs to be bias current through the input protection network to pull down the input sufficiently so the device can come out of saturation. However, the high source impedance is unable to furnish much bias current to begin with, and once the input is overdriven and the output saturates, the -INA input can be pulled up so that it now exceeds the common mode voltage range. In this situation, the differential pair can shut off, resulting in an indeterminate output state. If the indeterminate state leads to the output remaining saturated, then additional bias current is required to restore normal operation.

The solution

Figure 4 shows a simple solution to the problem in an instrumentation amplifier circuit using a three amplifier configuration. The LTC6090 is a single amplifier version of the dual LTC6091, and the LT5400-2 is a quad matched resistor network with ±75V operation, four 100kΩ resistors and better than 0.01% resistor matching.

Two 10kΩ resistors are added at the output to limit the worst-case output swing and prevent the feedback voltage from ever exceeding the input common mode range of the amplifier. Empirical tests show that above 20MΩ source resistance, there may not be adequate bias current to "free" the +INA input if it were to get "stuck." With lower source resistances, it is possible to pull down the +INA input after an overdrive event against the protection device leakage current that must be overcome (i.e., the high-Z input source retains control).

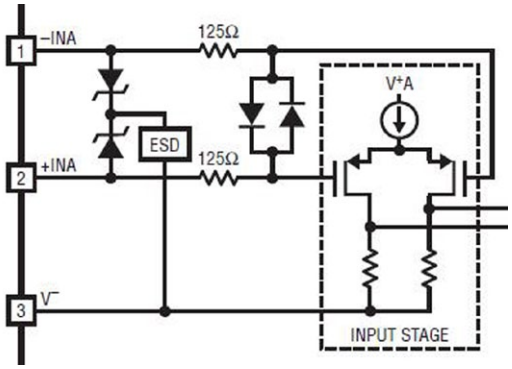


Fig. 3: LTC6091 50pA IBIAS amplifier input stage

Linear Technology offers a wide array of low bias current amplifiers with a wide range of performance specifications and power supply voltage requirements. These devices can help you realize your sensor design at optimum performance levels.

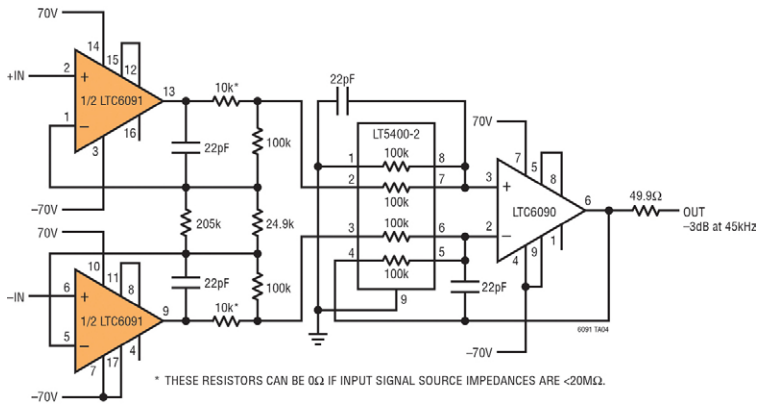


Fig. 4: 10kΩ resistors prevent amplifier output from saturating

Jon Munson is Applications Engineer at Linear Technology Corp – www.linear.com
Kevin Scott is Strategic Marketing Engineer at Linear Technology Corp.

Analog Aficionados dinner: littleBits' electronic project kits

By Tim McCune

One of my favorite parts of the annual Analog Aficionados dinners is the informal show-and-tell among designers. Among the items people have brought have been obscure and exceptional analog chips, 50-year-old one-inch wafers, and home-made wristwatches, scattered around the tables at David's Restaurant in Santa Clara. (The next such event is Jan. 31, 2016, see the Analog Aficionados website at www.analogaficionados.org for details.)

The coolest thing I saw last year was something Aficionado Geof Lipman brought, a box of small modular boards that connected to each other using magnets. Geof is the Director of Engineering at littleBits Electronics, Inc., a company based in New York City. I opened the box and soon found the hardest part of getting started was unwrapping the battery, and I was hooked in about 30 seconds.

For the past 50 years, any kids who have shown interest in electronics have gotten some variant of the "100-in-1" project box that uses springs and wires to connect parts into circuits. A great way to begin simple circuit design, but with these project boxes the possibilities exhaust quickly, and the concepts and components haven't advanced much.

Getting kids hooked on engineering is an important subject, and I wanted to learn more about littleBits. I caught up with Geof a while back to talk more about the project kits and how they'd come into being. He sent me some of their newest devices, and I passed them on to a friend for testing with his three kids, three, six and nine years old, hockey-playing youngsters who are miniature versions of the Hanson Brothers from the movie Slapshot.

Image courtesy of littleBits

The founder/CEO of littlebits is Ayah Bdeir, a thirty-something designer and entrepreneur originally from Montreal. After receiving her undergrad engineering degree from the American University in Beirut, Bdeir began working on new projects while earning her MS at the MIT Media Lab.

Lipman told me Bdeir did several concepts while at MIT, but what eventually became littleBits was the one that really took off. Bdeir completed the littleBits initial designs in true analog startup form, just herself and an intern doing the first work.

The modular electronics circuit building idea wasn't initially aimed at the education market, Lipman said. "The original concept here is when you're dealing with designers, industrial designers, sometimes people will be making models that they want to be functional models rather than just a sculpture that they build.

"So she started from the idea that people who don't understand electronics need better tools, because, for example, they can hook up an LED and accidentally burn it up in a second because they don't understand what's happening," he said. "They started as a way for designers to quickly prototype stuff like lights, sound, motion. It started with around ten designs that were completed before I joined the company. Then they added about 20 modules around the time I joined and I helped finish that batch up."

The company describes its work as a "library of modular components" that can be used to make a variety of circuits ranging from very simple to complex. The basic kit includes ten modules such as a DC motor, a switch, and a dimmer. More elaborate kits contain more electronic and mechanical items, as well as wireless interfaces to connect with the Internet and mobile devices. The design and construction of the kits is very high end, with prices ranging from around $99 for the basic one to $1,599 for "one of everything."

Tim McCune is President of Linear Integrated Systems Inc. - www.linearsystems.com

A key feature of the modules is the way they connect to each other, something that's covered in a patent application made by the company. The components only fit together in ways consistent with how electricity needs to flow, and the connections are secured by tiny magnets. Because of this the likelihood of damaging the components or connections, or even of making a bad circuit, is very small.

Many of our Analog Aficionados friends come up with great product ideas that never make it past tabletop or workbench demos, so I was pretty interested in how littleBits was able to generate funding and sales attention. Bdeir leveraged connections she had made at MIT and elsewhere and then showed the initial littleBits modules at conferences and exhibitions. She's a co-founder of Open Hardware Summit and received early support there and at Maker Faire.

Lipman joined the company as Employee No. 6 and helped expand the line of projects and modules. The company has been tripling in size every year for three years now and has over 100 employees. Most of the employees are engaged in creating internet-based tools to assist people building littleBits projects and also to support the community of users who exchange videos, information and assistance. The company's web site lists about 150 local littleBits chapters in 45 countries.

I looked at a couple dozen videos describing things littleBits users have designed, and the most interesting projects are the ones where users connect either physically or digitally to things beyond the littleBits modules. Some of the younger users connect the DC motors and servos to Lego constructions, while others rig projects to connect with cell phones and smart house components. "As a modern tech company, community is one of the big things that we have to worry about, and we put a lot of effort into it," Lipman said. "Like a lot of people I try to do things myself, but honestly when I'm trying to get up to speed quickly, I look at what other people have done." Some of his best product demonstrations have come from watching videos of what users have built, he said.

"If you're a responsible parent and you can help your child there's no safety problems with working with it in a mentored context," Lipman said. "They don't overheat, we've addressed the thermal issues pretty responsibly, they're hard to destroy from an ESD perspective, partially because of luck and partially because of design. And then we try to keep the corners not too sharp."

Feedback from the kids was excellent. I found that pretty much any kid can help build and enjoy projects with adult supervision. Sasha, the 9-year-old son of my friend and the self-appointed spokesman, said he enjoyed being creative with the littleBits kits. "My favorite thing is to do the hand buzzer and the tickle machine," Sasha said. "I like to make my own stuff."

"I really liked [littleBits] and I really liked how you could do multiple projects with one set," he said. "I liked the magnet connectors, and I really liked the synthesizer. I did most of the projects in the book, and I would like more parts to work with."

My conclusion after playing around with the kits, have my friend's kids work with them and viewing the online info is these kits will do a lot to get a broad range of people into some level of hardware design. A design community that brings in people who might have virtually no electronics experience is a valuable addition to other electronics design communities, such as diyAudio and of course the worlds of LTspice and other design tools. In a software/app/videogame-centric world, a kid actually creating a hardware device is a big step forward.

One useful addition to littleBits' support of this community, I believe, would be a simplified version of an LTspice-like circuit simulator to get kids into the world of circuit design as they would encounter in engineering classes.

MEMS fabrication on the cheap

By Julien Happich

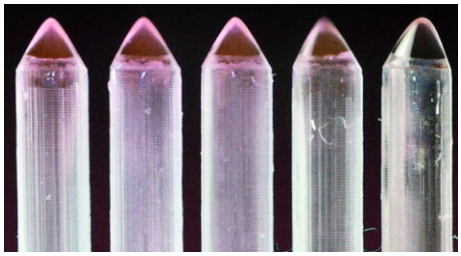
The mass fabrication techniques used for today's Microelectromechanical systems (MEMS) rely on costly semiconductor lithographic equipment. As for silicon chips, it will take a fairly large market to justify the production costs for any given device, and then commoditization is lurking.

Researchers at MIT's Microsystems Technologies Laboratories have demonstrated new ways to build MEMS on the cheap, not only enabling easy customization of the devices being produced, but also offering an alternative route to their manufacture with desktop-sized 3D printed fabs.

This new route to fabricating MEMS could yield new sensors and devices which otherwise may not have found a large-enough market to justify their full development from IP to final product using traditional processes.

The researchers' fabrication device sidesteps many of the requirements that make conventional MEMS manufacture expensive.

"The additive manufacturing we're doing is based on low temperature and no vacuum," says Luis Fernando Velásquez-García, a principal research scientist in MIT's Microsystems Technology Laboratories. "The highest temperature we've used is probably 60 degrees Celsius. In a chip, you probably need to grow oxide, which grows at around 1,000 degrees Celsius. And in many cases the reactors require these high vacuums to prevent contamination. We also make the devices very quickly. The devices we reported are made in a matter of hours from beginning to end."



External row of seven emitters that are part of a 49-emitter array. The scalloping on the exterior of the emitters, due to the layer-by-layer manufacturing, is visible. Source: Anthony Taylor and Luis F Velásquez-García (edited by MIT News)

The actual manufacturing technique relies on the use of dense arrays of emitters that eject microscopic streams of fluid when subjected to strong electric fields.

To build gas sensors, Velásquez-García and Anthony Taylor, a visiting researcher from the British company Edwards Vacuum, used so-called "internally fed emitters."

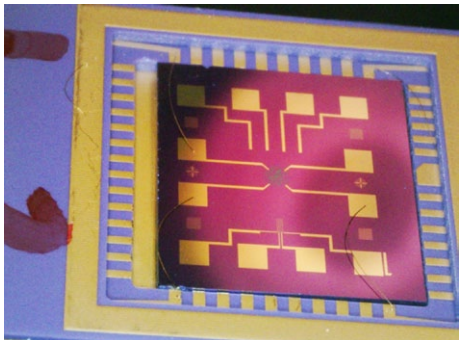
These are emitters with cylindrical bores that allow fluid to pass through them. The researchers used a fluid containing tiny flakes of graphene oxide, to be sprayed in a prescribed pattern on a silicon substrate.

The fluid quickly evaporated, leaving a coating of graphene oxide flakes only a few tens of nanometers thick.

The flakes are so thin that interaction with gas molecules changes their resistance in a measurable way, making them useful for sensing.

According to Velásquez-García, the gas sensors obtained were as precise as a commercial product costing hundreds of dollars, while being faster and built for only a few cents.

In their first implementation, the electrospray emitters used by Velásquez-García and Taylor had been built using conventional semiconductor processes. But in a second study published in the December issue of the Journal of Microelectromechanical Systems, Velásquez-García reports using an affordable, high-quality 3-D printer to produce plastic electrospray emitters whose size and performance match those of the emitters that yielded the gas sensors.



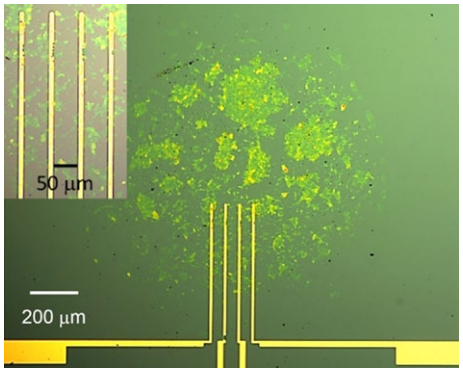
A completed chip with a wired graphene oxide gas sensor. The graphene oxide film is the greenish dot covering the electrode structure. Source: Anthony Taylor and Luis F Velásquez-García

Not only were the researchers able to make the electrospray devices more cost-effective, 3-D printing allowed them to customize the devices for particular applications, improving the micronozzles from one iteration to the next within days.

Effectively, they were able to build new MEMS out of their custom MEMS fab desktop. Another big advantage is that the low process temperature allows sensor designers to deposit materials that would not be compatible with high-temperature semiconductor manufacturing, such as biological molecules with specific markers.

The new fabrication technique could open up new application fields for MEMS while taking more IP to viable commercial products.

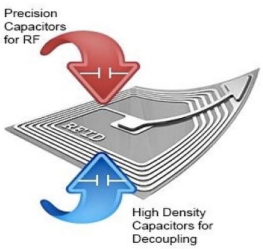
"In some cases, MEMS manufacturers have to compromise between what they intended to make, based on the models, and what you can make based on the microfabrication techniques," Velásquez-García explained. "Only a few devices that fit into the description of having large markets and not having subpar performance are the ones that have made it."



Optical micrograph of a fabricated conductometric graphene oxide gas sensor. The inset (top left corner) shows a close-up view of the active area of the sensor. Source: Anthony Taylor and Luis F Velásquez-García.

Ipdia makes thin silicon caps

3D silicon passive components provider Ipdia (Caen, France) has developed a range of low profile capacitors with electrostatic discharge (ESD) performance up to 8kV. The capacitors are suitable for use in smart cards and RFID tags and in other applications where integration and antenna matching play key roles. The LPSC range targets antenna matching, RF filtering and decoupling of active die, in applications with height and volume constraints. The RFID 0402 capacitor range is 100-microns thick while providing stability over the specified voltage up to 150°C. The range covers values from 10pF up to 330pF, with the same thermal coefficient as standard RFID ICs and with proven assembly methods such as flip-chip and wirebonding. Furthermore, the capacitor range has been tuned to reach a series resonant frequency (SRF) higher than 1.2GHz, allowing antenna tuning from 13.56MHz up to 800/900MHz applications.



Ipdia
www.ipdia.com

Highest-performing audio op amp, claims TI

Citing lowest distortion and noise, high linear output current, and low power, Texas Instruments says its latest audio amplifier pushes the boundaries for professional and portable audio. The OPA1622 is the newest addition to the company's Burr-Brown Audio line and is the next generation of the widely adopted OPA1612. The OPA1622 delivers high output power of up to 150 mW and extremely low distortion of -135 dB at 10 mW, enabling the highest performance for professional audio equipment. The OPA1622's small size, low power consumption and low distortion can deliver high-fidelity audio in portable devices such as headphone amplifiers, smartphones, tablets and USB audio digital-to-analogue converters (DACs).The OPA1622 op amp, TI adds; - Pushes the boundaries of audio quality: Headphone amplifier designers can take advantage of its low total harmonic distortion (THD) of -135 dB at 10-mW output power into a 32-Ω load – a claimed 12 times better than the nearest competitor. It also delivers maximum output power of up to 150 mW before clipping while maintaining the lowest THD and noise (THD+N), providing a clean signal path for professional audio applications. - Optimised for high-fidelity portable audio devices: Consumes quiescent current of 2.6 mA per channel and delivers high linear output current of 80 mA rms in a 3 x 3-mm dual flat no-lead (DFN) package. Increased power-supply rejection ratio (PSRR) of -97/-123 dB at 20 kHz enables low distortion from switching power supplies with no low-dropout regulator (LDO), saving board space without compromising audio performance. The OPA1622's ground-referenced enable pin is directly controllable from the low-power processor's GPIO pins without level-shifting circuits.

Texas Instruments
www.ti.com

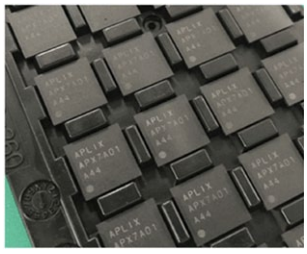
Startup launches switch-mode op amps, ADCs

Seamless Devices Inc. (San Jose, Calif.), a startup spun out of Columbia University, New York, in 2014 has introduced its first products, a set of analog front-end circuits for use in LTE, WiFi and microwave applications. Seamless was formed by Professor Peter Kinget and former student Jayanth Kuppambatti to apply developments in switched-mode analog signal processing across a broad range of applications and making use of nanoscale manufacturing processes. Seamless Devices is a semiconductor IP company, following a similar business model to ARM Holdings Ltd., and is owned by Allied Minds plc. Allied Minds is private equity-funded incubation company that forms, funds, manages and builds startups based on early-stage technology developed at US universities and laboratories. Seamless Design's switched-mode operational amplifier (SMOA) can address high frequency signals using leading-edge transistors and therefore is a candidate technology for adding analog circuits for SoCs. The company claims that its first set of AFEs make it easier for architects of signal processing systems to address the trade-off between performance quality and power usage in electronic devices. The company is introducing a portfolio of products, including analog-to-digital converters (ADCs), analog filters, and a programmable gain amplifier. "These products demonstrate our SMOA's potential to enable a new class of performance," said Roger Yang, general manager of Seamless Devices, and a vice president at Allied Minds. The company's ADCs offer 80MHz bandwidth from 0.9V operation, automatic background PVT calibration and available in 28nm CMOS processes.

Seamless Devices Inc.
www.seamlessdevices.com.

Former games company offers analog IC for IoT

Aplix IP Holdings Corp. (Tokyo, Japan), a public company that previously made games software and video animation, has re-invented itself as an Internet of Things company with the introduction of an analog interface IC for the smart home. Aplix claims that this analog IC can be used to connect a variety of home and office appliances, such as thermostats, water detectors, heaters and motors, to the Internet. Aplix is also developing relevant digital logic and plans to supply its analog and digital circuitry in the form of intellectual property. A single-chip IoT solution (SoC) can be realized by combining Aplix IP with Bluetooth semiconductor IP and processor IP. Aplix said it plans to license its analog and digital design IP library to semiconductor companies and foundries. BiCMOS 44pin QFN or 64pin QFP 0.5mm pitch that provides 3V power regulation; 8 or 16 channel comparator input; an 8 or 16 channel voltage level shifter; 4 channel LED driver and 4 channel analog switch, according to the company's website. But it appears to be part of a long-term plan to license the makings for a IoT interface ICs. The company has published a roadmap that extends to 2018.



Aplix IP Holdings Corp.
www.aplix-ip.com

Kandou SerDes capable of 1Tbit/s

The Glasswing SerDes core in development at startup Kandou Bus SA has been tested and demonstrated the "capability of achieving" 1Tbit/s chip-to-chip at less than 1W of power consumed. Kandou's technology is based on signaling method called Chord Signaling in which correlated signals are sent across multiple wires. The version of Chord Signaling employed in Glasswing, CNRZ-5 coding, delivers 5 bits over 6 wires for a total bandwidth of 125Gbps. The link achieves a BER of <10^-15 at the targeted data rate of 25GBaud and can support channels up to 12mm in length (die-to- die insertion loss up to 6dB) at full rate and 24mm at half rate. The link has also proven to be robust under stress including overclocking up to 30GBaud, temperature testing from 0° to 100°C, and running full rate up to 24mm. Measured power for a single instantiation of the link is 1.1pJ/bit and in a quad configuration would drop to 0.97pJ/bit. Through the use of a bi-directional version of Glass wing 2Tbps of bandwidth can be achieved using only 320 signal pins and standard bump pitches, the company said. The Glasswing link IP is delivered as a hard IP and licensed customers receive: data sheet and application notes, channel compliance guidelines, standard integration views (GDS, LEF, verilog, .lib), production test support, Spice models and Kandou proprietary KEYE and TAU modelling tools.

Kandou Bus SA
www.kandou.com

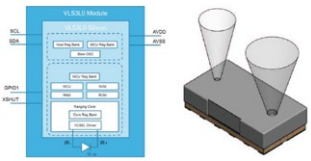
DACs with NVM retain settings in power-off

The low-power, 8-/10-/12-bit, single and dual-channel MCP-48FXBXX digital/analogue converters with SPI have optional integrated EEPROM to reduce microcontroller overhead: shutdown modes reduce current consumption for power-critical applications. The six-member MCP-48FEBXX DAC family offers integrated EEPROM to save DAC settings at power-down, while the MCP-48FVBXX family provides lower-cost alternatives for applications that do not require integrated memory. These low-power, single and dual-channel DACs feature 8-, 10- and 12-bit resolution, a Serial Peripheral Interface (SPI), and are available in 10-pin MSOP packages. Examples of their wide range of applications in the consumer, industrial, automotive and other markets, includes set-point/offset trimming, sensor calibration, instrumentation, and motor control. The integrated EEPROM option enables DAC settings to be restored at power-up and reduces microcontroller overhead, while the various shutdown modes significantly reduce the device current consumption for power-critical applications. These devices feature low Differential Nonlinearity (DNL) error to sustain monotonic output and low Integral Nonlinearity (INL) error for better linearity. They can operate in extended-temperature conditions.

Microchip
www.microchip.com

Time-of-flight ranging sensor for cameras, robotics, IoT

Promising to 'revolutionise mobile-camera Performance and enable new applications in robotics and IoT, ST Microelectronics' FlightSense VL53L0 low-power, miniature sensors



can be used for fast autofocus in smartphones, for proximity sensing, and object detection This is ST's second-generation laser-ranging sensor based on its FlightSense technology. VL53L0, can range faster, over longer distances, and more accurately. In a form factor of 4.4x2.4x1mm, ST says the VL53L0 is the smallest ToF (Time-of-Flight) module available, and the first to integrate a 940 nm VCSEL (vertical cavity surface-emitting laser) light source, a SPAD (single-photon avalanche diode) photon detector, and an advanced microcontroller to manage the complete ranging function. Being the market's first module to use light emitted at 940 nm, coupled to leading-edge infrared filters, the VL53L0 maximises ambient light immunity and is now invisible to the human eye. The embedded microcontroller and digital algorithms minimise both the host processing and system power consumption in the final application. The VL53L0 is able to perform a full measurement operation in one image frame, typically less than 30ms, at distances beyond 2m.

STMicroelectronics
www.st.com

360° programmable magnetic angle position sensor

A1335 from Allegro MicroSystems Europe is a 360° contactless high-resolution programmable magnetic angle position

sensor IC designed for use in digital systems in automotive and related applications involving rotating shaft sensing. It is available as single or dual independent die in a single package. The device has a system-on-chip (SoC) architecture with a front end based on circular vertical Hall technology and programmable microprocessor-based signal processing. It supports multiple communication interfaces including I²C, SPI (Serial Peripheral Interface), and SENT (Single Edge Nibble Transmission). In addition to providing 360° angular measurement, the A1335 provides two options for on-chip linearisation: harmonic linearisation to handle applications that require side-shaft magnetic configurations; and segmented linearisation for scaling angle measurement applications requiring less than 360° of motion (so-called "short stroke" applications). It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible programming of calibration parameters.

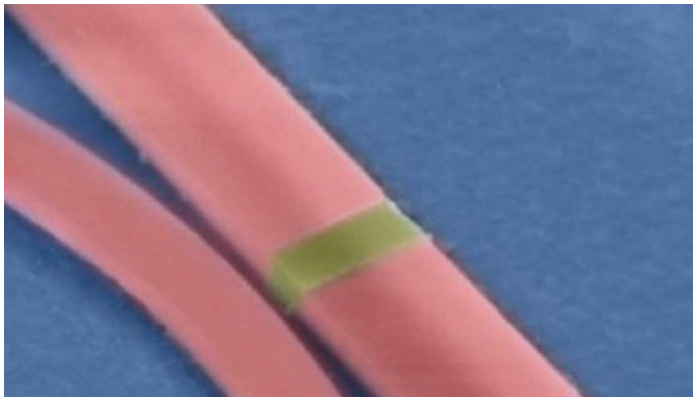
Allegro MicroSystems
www.allegromicro.com

Optical phase-change memory can increase bandwidth

By Peter Clarke

A research team from the universities of Oxford and Muenster has developed a phase-change, non-volatile memory that is programmed and read using light and which could be interfaced to conventional electronic processor for higher bandwidth.

The device is based on the classical chalcogenide material $Ge_2Sb_2Te_5$ (GST) that is also used in compact discs and DVDs and which can adopt either an ordered crystalline or disordered amorphous state.



A scanning electron microscope image of optical memory GST layer, highlighted in yellow, on top of the silicon nitride waveguide, highlighted in red. Source: Oxford University.

In a paper published in Nature Photonics, the researchers describe how they included a small patch of GST on top of a silicon-nitride waveguide and used an intense pulse of light causing the thin film to melt. On cooling it assumes an amorphous structure. A less-intense pulse and slower cooling puts the film into a crystalline state and light with much lower intensity can be used to read the state of the film, the researchers report.

"There's no point using faster processors if the limiting factor is the shuttling of information to-and-from the memory – the so-called von-Neumann bottleneck," said Professor Harish Bhaskaran, in a statement. Professor Bhaskaran is the Oxford engineer who led the research along with Professor Wolfram Pernice from the University of Muenster.

Using optical transport can be used to transfer data but carries an overhead if the optical signals need to be converted back into electronic signals at the point of storage. By making the memory system optical this overhead has been reduced. Researchers have tried to create this kind of photonic memory before, but the results have always been volatile, requiring power in order to store data, according to Oxford University.

"This is the first ever truly non-volatile integrated optical memory device to be created," said Carlos Rios, one of two lead authors of the paper along with Matthias Stegmaier. "And we've achieved it using established materials that are known for their long-term data retention — GST remains in the state that it's placed in for decades." The researchers have also shown that it is possible to use wavelength multiplexing – sending multiple light pulses of different wavelengths at the same time – it is possible to write and read to the memory at the same time. "In theory, that means we could read and write to thousands of bits at once, providing virtually unlimited bandwidth," said Professor Pernice, in the same statement.

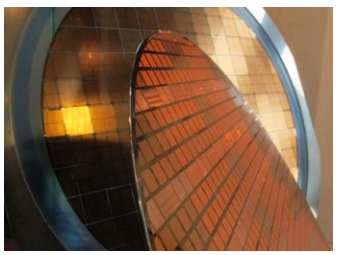
The research also report that different light intensities can be used to accurately and repeatedly create different proportions of amorphous and crystalline within the GST film. When lower intensity light pulses are sent through the waveguide the researchers were able to detect these different mixes by changes made to the transmitted light, allowing the possibility of reading up to eight different memory levels allowing the storage of 3 bits of data per memory site.

Professor Bhaskaran said the team has demonstrated novel functionality using proven existing materials and the optical bits can be written with frequencies of up to one gigahertz. The team is now working on an electro-optical interconnect, which will allow such optical non-volatile memory chips to connect with other components using light, rather than electrical signals.

The paper 'Integrated all-photonic nonvolatile multi-level memory' was published in Nature Photonics.

Fastest 64 Mb Quad SPI NOR flash runs in extended temperature range

The FS-S family of devices from Cypress provide high read bandwidth to enable faster access times in high-performance embedded systems and now the company has introduced a 1.8V, 64 Mb NOR flash memory with a Quad Serial Peripheral Interface (Quad SPI).The Quad SPI interface is combined with the highest read bandwidth and fastest program time while enabling a small PCB layout. The device is sutiable for high-performance applications, such as video game consoles, Advanced Driver Assistance Systems (ADAS), automotive instrument clusters and infotainment systems, networking equipment and set-top boxes.The 64Mb FS-S Quad SPI NOR Flash memory uses an 80-MHz Double Data Rate (DDR) mode to deliver read bandwidth of 80 MBps and enables the fastest program execution for high-performance systems.



Available in 8-lead SOIC and 24-ball BGA packages, the device provides a 0.475-msec program time per 512 bytes, increasing manufacturing throughput and enabling new data to be written quickly. For battery-powered applications, the memory extends battery life by providing low standby current and a deep-power-down mode. The FS-S NOR Flash family offers AEC-Q100 automotive qualification and supports an extended temperature range of -40°C to +125°C.

Cypress
www.cypress.com

Flash, STT-MRAM and resistive RAM: they all come with different challenges

By Arnaud Furnemont

Research in memory is really exciting these days: in parallel you have the scaling of classical memories (SRAM, DRAM, Flash) and the emergence of new memories capable of enabling new applications or even new system hierarchies. At imec, we mostly focus on three concepts which all come with different challenges.

First is Flash, and specifically 3D NAND. Here it's the integration challenge that is keeping us all busy. Before, the focus was on device scaling, but now it's all about stacking more layers. Last year, we explored new materials for the channel (e.g. III-V channel in 3D NAND) and for the trapping layer (YAlO instead of SiN), in parallel with device reliability characterization and modelling.

Another important memory type is STT-MRAM where a complex magnetic stack makes the scene. Focus here is on choosing the right material combination and developing the perfect stack (with perfect interfaces!). Over the last years, imec made a lot of progress to build a good stack. But even more challenging is the patterning of this multi-layers structure without affecting the magnetic properties of the device. Very recently we were able to demonstrate 45nm devices with good performance. Tool suppliers are improving the etch platforms and I expect STT-MRAM as embedded memory in the foundries by 2017 and as standalone memory by 2020. In the latter case, more scaling is necessary and this implies more etch issues which will have to be solved.

Thirdly, we explore resistive RAM. The challenge for this type of memory is picking the right combination out of the numerous kinds of stacks and materials. And to do this, you need a fundamental understanding of what happens inside each stack. Imec has developed in depth characterization and modelling on OxRAM and CBRAM memories, expected to be used in embedded applications. Globally, RRAM suffers from a

trade-off between write energy and stability. VMCO is another RRAM variant developed at imec to break this trade-off. To be competitive in standalone applications, RRAM will also need to be combined with a selector, which requires again material selection and benchmarking. This is a role that imec is willing to take on for its partners.

Finally, there is also a high-level challenge that the memory researchers and developers are facing. It's the changing landscape in which emerging memories have more and more impact on the system architecture. Before, the system hierarchy was built with the memory technologies that were available. In the future it might be the other way around: the system architects will tell us what to develop. A closer collaboration between the device team and system architects is therefore indispensable. Imec's memory 'insite' activity will tackle this challenge.

Arnaud Furnemont is memory department director, MRAM and Flash program director at imec – www.imec.be

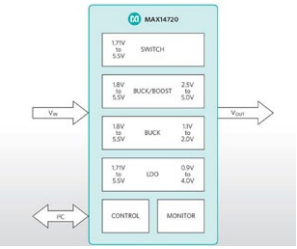
15nm e•MMC NAND Flash memory meets AEC-Q100 specifications

Toshiba Electronics Europe has launched a new range of 15nm e•MMC NAND Flash memory for automotive infotainment systems as well as industrial applications. The automotive e•MMC supports a wide operating temperature range of -40 to 85°C and meets AEC-Q100 specifications as well as adhering to PPAP requirements. The chips are claimed to be among the world's smallest and are available in an 11.5x13mm package that is fully compliant with the latest JEDEC e•MMC standard. The new line-up of single-package embedded NAND flash memories includes densities from 8GB to 64GB. Each device integrates a controller to manage basic control functions for NAND applications.

Toshiba Electronics Europe
www.toshiba.semicon-storage.com

Power management chip targets non-rechargeable IoT

The MAX14720 power management integrated circuit (PMIC) from Maxim Integrated Products will help designers optimize power and battery life for wearable medical/fitness and IoT applications running on primary cells. The MAX14720 PMIC is well suited for non-rechargeable battery (coin cell, dual alkaline) applications where size and energy efficiency are critical. In addition, an electronic battery seal extends shelf life by effectively disconnecting the battery prior to initial power-up. Integrating the functionality of five discrete devices—power switch, linear regulator, buck regulator, buck-boost regulator, and monitor—the MAX14720 reduces the bill of materials (BOM) and allows for much smaller form factor designs. While most battery PMICs operate from 3V, the MAX14720 runs from a primary cell and operates down to 1.8V. Its low quiescent current IP is critical for wearable applications because it can extend the runtime of the system significantly. The chip comes in a 25-bump, 0.4mm pitch, 2.26x2.14mm wafer-level package (WLP) and is specified over the -40-degree Celsius to 85-degree Celsius temperature range.



Maxim Integrated
www.maximintegrated.com

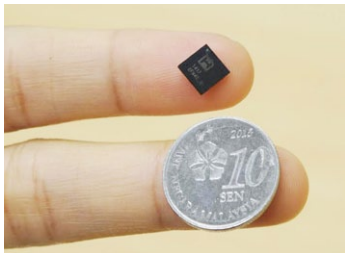
Self-aligning, floating board-to-board connector offers ±0.6mm margin

Hirose has designed a board-to-board connector with a highly reliable floating contact mechanism and self-alignment structure that simplifies assembly. Providing ±0.6mm floating in the X and Y axis directions, the FX20 Series absorbs mounting misalignment from multiple stacking connectors as well as PCB shrinkage caused by high temperatures. Well suited for industrial and vehicle applications, the FX20 Series has a highly reliable double beam contact structure that provides high shock and vibration resistance. Each contact beam has a different vibration characteristic and a different contact force, which widens the frequency range and reduces resonance. In this unique design, the first beam has a 0.5N contact force, while the second beam has a 0.35N contact force. The FX20 Series is resistant to sulfur dioxide, and operates in environments up to 105 degrees C, with thermal shock protection from -40 degrees C to +85 degrees C for up to 1000 cycles. The double beam contact structure also provides self-cleaning functionality. The connector has a compact 0.5mm pitch design that delivers a 0.5 Amp current per pin capacity, it requires only 120 positions to carry 60 Amps versus 200 positions from competing technologies. The connector is offered in a parallel stacking version with stacking heights of 15, 20, 25 and 30mm, as well as a right-angle mating type.

Hirose Electric
www.hirose.com

Motion controller IC implements FOC in silicon

The MCGP021 or Green Motion Controller (GMC) designed by Malaysia's national research and development agency in information and communications technology, MIMOS, together with two local collaborators, My Technology and Emerald Systems, could potentially replace existing controllers for Permanent Magnet Synchronous Motors (PMSM). Thirteen joint Intellectual Properties were generated in developing the solution, which took two years to develop. While traditional solutions for controlling Permanent Magnet Synchronous Motors (PMSM) motor use software written for a microcontroller or microprocessor, MIMOS' MCGP02I motion controller solution uses a new design approach in which complex mathematical calculations required for Field Oriented Control (FOC) of PMSM motors are directly implemented in silicon, with logic gates. Because when using the MCGP02I, there is no need to write firmware to implement the complex FOC algorithm, total development cost of the system can be greatly reduced. The programmability of all control parameters enables maximum flexibility and the quick design of control systems. The MCGP02I comes in a 40-pin small footprint QFN package with an integrated on-chip oscillator, ADCs, voltage references and regulator.



MIMOS
www.mimos.my

FTDI enriches 8-bit FT51A MCU with comprehensive ecosystem

In order to support its FT51A microcontroller unit (MCU), which is now in full production, FTDI Chip has introduced an array of board levels products. The objective of the FT51A-EVM evaluation module is to furnish engineers with a multitude of different functions through which they can get a better understanding of the FT51A MCUs application parameters - in particular its suitability for multi-sensor circuits. The module incorporates a 20x2 character LCD display (with an RGB backlight) plus a series of different sensor mechanisms through which various forms of data can be acquired. There is a heart-rate monitor (with filtered and amplified analogue output), a force sensitive resistor (which can measure the pressure applied by the users finger) and a SPI-enabled temperature sensor. The upstream and downstream USB ports permits cascading of multiple units. The module comes preloaded with dedicated firmware - allowing the full scope of the FT51As functionality to be benefited from while avoiding the need to create any code. Provision has been made within the modules IOs for communication with FTDIs FT800 Embedded Video Engine (EVE) modules, so that more sophisticated human machine interfaces can be added if necessary.

FTDI Chip
www.ftdichip.com

Bridge chip brings Ethernet AVB to infotainment

Toshiba Electronics Europe has introduced an automotive-grade Ethernet bridge solution for in-vehicle infotainment (IVI) and other automotive applications. The TC9560XBG supports standards such as IEEE 802.1AS and IEEE 802.1Qav, generally referred to as Ethernet-AVB. The Ethernet-AVB standard enables stable, reliable multimedia transmissions, making it suitable for IVI and telematics. The device has been developed under the ISO/TS 16949 and APQP automotive design quality system and is being AEC-Q100 qualified to guarantee quality and performance in rigorous automotive environments. The TC9560XBG is housed in a 10 x 10mm LFBGA package. When connected to an application processor or other system-on-chip (SoC) host, the TC9560XBG allows the host device to deliver audio, video, and other data through the 10/100/1000 Ethernet network in an automotive environment. Connection to the host is via PCI Express (PCIe), HSIC or Time Division Multiplex (TDM)/I2S for audio traffic. The chipset's RGMII/RMII/MII interface connects to the Ethernet switch or PHY device, and both AVB and legacy traffic are supported. An on-chip ARM Cortex-M3 processor performs system control and management. In addition to the functionality offered by the TC9560XBG Ethernet bridge solution, Toshiba also is introducing the TC9560AXBG, which also provides automotive OEMs with access to CAN-FD functionality.

Toshiba Electronics Europe
www.toshiba.semicon-storage.com

0.67-inch 4K UHD DLP chip supersizes projection displays

Texas Instruments has released a 0.67-inch 4K UHD chip for home theater, business and education projection displays based on its proven DLP Cinema technology. The DLP 4K UHD chipset combines the fast switching speed of the digital micromirror device (DMD) with advanced image processing. The integrated MEMS solution delivers more than 8 million pixels to the screen with just 4 million mirrors. Each mirror is capable of switching over 9,000 times per second, creating two distinct and unique pixels on the screen during every frame to deliver full 4K UHD resolution. The inherent one-chip DLP system alignment enables the color integrity of the content to be maintained without blurriness between colors. With a small, 0.67-inch DMD that is similar in size to the DLP 0.65-inch 1080p chip, customers can have access to more affordable 4K UHD solutions in settings ranging from the home theater to the boardroom to the classroom.

Texas Instruments
www.ti.com/dlp

400W front-end AC/DC modules maximise power density

Vicor has added to its range of high density AC-to-DC front-end modules with isolation and power factor correction, packaged in a chassis-mountable module format, and providing up to 400W of isolated 24 or 48 VDC. These PFM AC-DC front-end modules use Vicor's VIA package, maximising cooling performance and versatility in converter mounting. They have universal AC input (85 – 264 VAC), power factor correction, and a fully isolated 24 VDC or 48 VDC output, and deliver 400W of isolated, regulated, DC output power at efficiencies up to 93%. This equates to 127 W/in³ (8 W/cm³) in the 9 mm profile VIA package, for use in industrial, process control, telecommunications, office equipment, test and measurement, LED lighting and other "off-line" applications. These new units integrate a full range of front-end functions required by contemporary AC line-operated power systems -- transient and inrush current protection; input power factor correction; input to output isolation; and a regulated SELV (Safety Extra Low Voltage) DC output -- and meet international safety and regulatory agency standards for isolation, conducted emissions, power factor correction, and susceptibility to AC line transients, flicker, interruptions and surges.

Vicor
www.vicorpower.com

Programmable LED light source for camera calibration

Using the GL OptiLight LED 127 CLC, camera manufacturers no longer need to use complex color checking targets on their production lines. The OptiLight can provide two identical selectable color temperature sources (including D65 and D50) and several levels of radiance for calibrating both front and back cameras simultaneously. Since the OptiLight provides near-perfect replication of light sources like D50, D65, D75, A or TL 84 it can be used as a precise calibration reference for many types of optical instruments in manufacturing lines, laboratories, and test facilities. With closed-loop calibration control using a high-accuracy photodiode and thermal stabilization, the OptiLight is claimed to achieve extraordinary colorimetric stabilization that suits critical production requirements. GL OptiLight LED 127 CLC is designed with analog closed-loop calibration using a built-in high-accuracy photodiode and a compact integrating sphere, providing ideal source homogeneity. The internal LEDs are controlled via an automated multilevel calibration procedure without requiring any external measurement device. The unit can be used to create almost any color source when controlled by a PC via USB connection or set with the built-in control panel. The spectral range available is from 385 - 750 nm and the luminance range from 100 - 3000 cd/m.

Saelig
www.saelig.com

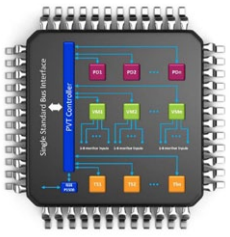
Handheld oscilloscope offers the performance of a lab instrument

Rohde & Schwarz is offering a handheld oscilloscope with the functionality and touch and feel of a state of the art lab oscilloscope. Scope Rider combines five instruments in a compact format, and its rugged design makes it perfect for mobile installation and maintenance work. The instrument features isolated input and communications interfaces. It meets CAT IV standards and can carry out measurements on low voltage installation sources up to 600 V. With an acquisition rate of 50,000 waveforms per second, a 10 bit A/D converter developed by Rohde & Schwarz and a maximum bandwidth of 500 MHz for the analog input channels, this portable oscilloscope clearly outperforms comparable instruments. Scope Rider integrates five functions to offer a level of versatility not found in any other instrument. It is based on a high performance oscilloscope featuring a precise digital trigger system, 33 automatic measurement functions, mask test and XY diagram mode. Plus, Scope Rider can function as a logic analyzer with eight additional digital channels, as a protocol analyzer with trigger and decoding capability, as a data logger and a digital multimeter. This wealth of functions makes it ideal for a wide range of tasks. The handheld oscilloscope is the first to be equipped with a large format capacitive touchscreen, allowing it to be operated as intuitively as a tablet PC.

Rohde & Schwarz
www.rohde-schwarz.com

On-chip process, voltage and temperature sensing controller IP ready for 28nm

Moortec Semiconductor Limited, a provider of embedded die monitoring IP solutions for advanced nodes, has released a PVT controller that provides a single standard interface to its embedded Process, Voltage and Temperature (PVT) sensing Sub-System. On-chip PVT monitoring is now a key consideration for 28-nanometer (nm) and FinFET technology based designs. Higher accuracy monitors embedded within SoC designs enable a greater opportunity for dynamic performance optimisation, either for lower power or higher data throughput as well as offering greater device reliability. Sensing die temperature, detecting logic speed and monitoring voltage supply levels can be used intelligently to vary system clock frequencies and the voltage levels of supply domains. A benefit of embedded thermal monitoring in particular is to enhance device reliability and life-time by assessing the electro-migration effects of hot spots within the chip. A key aspect is that PVT data collection can be applied to each and every device, either during production or 'in-the-field'. Moortec believe that strategies adopted by IC designers over the coming years will be heavily influenced by the analysis of data harvested from in-chip monitors.



Moortec Semiconductor
www.moortec.com

Go beyond the "Rails"!

This month Maxim Integrated is giving away 10 of its new break-through "Beyond-the-Rails™" precision, low-noise, low-drift, MAX44267 dual operational amplifier evaluation kits, worth approximately 50 USD each. The kit showcases the MAX44267, a precision, low-noise, low-drift dual operational amplifier that offers true-zero output which allows the output to cross zero, maximizing the dynamic range of an ADC and increasing resolution. In addition, the input common-mode range extends from +13.5V down to -12V. Delivered in a 14-pin TSSOP package, the MAX44267 integrates charge-pump circuitry that generates the negative voltage rail in conjunction with external capacitors. This allows the amplifier to operate from a single +4.5V to +15V power supply, but it is as effective as a normal dual-rail ±4.5V to ±15V amplifier. Easy to set up and run, the MAX44267 evaluation kit will save you space and cost by eliminating the need for isolating a negative supply rail. The EV kit circuit is preconfigured as non-inverting amplifiers, but can be adapted to other topologies by changing a few components. It can be connected directly to bipolar input sensors and is well suited for Programmable Logic Controller front ends.

Check the reader offer online at
www.electronics-eetimes.com

Hi-Bri LEDs allow exact lighting level

Semiconductor supplier Rohm has succeeded in creating an LED type that excels through extraordinarily low individual brightness variation. This results in highly homogeneous light yield, making the LEDs ideal for automotive lighting applications. The need to reduce brightness variations is increasing as a greater number of applications and devices, particularly in the automotive and industrial sectors, are demanding improved consistency when configuring multiple LEDs side-by-side. However, up to now it has been difficult to minimize brightness variations during the manufacturing process. Conventionally, users were able to only narrow down the number of ranks from around 4 to 2-3, which still required sorting and the use of different resistors to match each rank, increasing the number of man-hours required along with inventory management. In response, the SML-D15 series was developed using a comprehensive, highly integrated manufacturing system, allowing Rohm to surpass the limits of conventional LED production. As a result, high-accuracy brightness is achieved and brightness variations reduced by 75%. This makes it possible to provide a single rank of brightness, significantly lightening design load. In addition, by optimizing the LED element Rohm was able to improve brightness by up to 3x over conventional products, delivering class-leading brightness in the 1608 size (1.6x0.8mm).

Rohm
www.rohm.com/eu

Half-bridge evaluation board simplifies GaN transistor testing

A manufacturer of gallium nitride power transistors, GaN Systems has launched a half-bridge evaluation board which

demonstrates the performance of its GaN enhancement mode power semiconductors in real power circuits. The fully functional GS66508T-EVBHB Evaluation Board is easily configured into any half-bridge-based topology, including synchronous boost and buck conversion modes, as well as pulsed switching to evaluate transistor waveforms. Accompanied by a Quick Start Instruction Guide and YouTube video links, the Evaluation Board can be installed and used in minutes. Each development kit comes with full documentation, including Bill-of-Materials component part numbers, PCB layout and thermal management, and a gate drive circuit reference design to help system engineers develop their products. Designed to provide electrical engineers with a complete working power stage, the evaluation board consists of two 650 V, 30 A GS66508T GaN FETs, half-bridge gate drivers, a gate drive power supply, and heatsink. The GS66508T high power transistors are based on GaN Systems' proprietary Island Technology® and belong to its 650 V family of high density devices which achieve extremely efficient power conversion with fast switching speeds over 100 V/nS and ultra-low thermal losses. The 30 A / 50 mΩ GS66508T GaN power transistors are top-side cooled, and feature near chip-scale, thermally-efficient GaNPX packaging. At 1.5 kW, this device's power conversion efficiency is rated at 98.7%, a value which can be reproduced in the owner's lab.

GaN Systems Inc.
www.gansystems.com

Startup offers all-in-one 2G/3G/4G front-end

Morfis Semiconductor Inc. (Irvine, Calif.), a startup founded in 2013, has announced it has developed a single-die flip-chip RF front end to support all 2G/3G/4G LTE frequency bands. The chip does this without compromising efficiency and linearity the company claims in a press release.

The company plans to exhibit at the Consumer Electronics Show to take place in Las Vegas in January and to show there a multi-mode, multiband power amplifier and its RF front-end. Morfis is sampling special customers and mass production is scheduled to start in 2Q16. The company staff has been drawn from other RF companies in the area according to LinkedIn filings. Charlie Chen is CTO and was previously engineering fellow and director of engineering at RF Axis Inc. (Irvine, Calif.). Yun Shi, who was previously with Qualcomm, is director of operations and Zhan Xu, previously with TriQuint Semiconductor, is an engineering fellow at Morfis.

Morfis Semiconductor Inc.
www.morfis.com

Advanced Bluetooth Smart remote reference design

Available now, the nRFready Smart Remote 3 is a complete state-of-the-art hardware and software Bluetooth Smart reference design featuring voice input control, 39 programmable buttons, 6-axis motion sensing, and multi-touch trackpad The reference design that is said to make the development of advanced Bluetooth® Smart remotes as easy as clicking on a list of check box options, and so minimizing time-to-market and unnecessary design risk. Targeting remote control OEMs/ODMs and smart TV, set-top box, and digital media device manufacturers, the nRFready Smart Remote 3 reference design is designed to deliver a rich, intuitive, and engaging end-user experience. It employs state-of-the-art voice input and speech recognition control, a 6-axis motion sensing 'Air-mouse', multi-touch trackpad technology, plus 39 developer-programmable buttons and legacy IR hardware support (to control IR-only products). In operation, the nRFready Smart Remote 3 reference design employs Nordic's nRF51822 System-on-Chip (SoC) and so is designed to work as an add-on for Nordic's existing nRF51 Development Kit (DK).

Nordic
www.nordicsemi.com

DISTRIBUTION CORNER

RFMW Ltd and Southwest Antennas strike distribution agreement

RFMW Ltd. and Southwest Antennas of San Diego have announced a distribution agreement whereby the specialized distributor will stock Southwest Antennas' RF and microwave antennas and accessories operating in frequencies up to 8.5 GHz, with capabilities beyond 20 GHz. Under the agreement, RFMW is franchised worldwide for Southwest Antennas' full range of antenna related products which includes accessories such as antenna mounting solutions, block downconverters, low noise amplifiers, and filter modules. Southwest Antenna products are designed, built, and qualified at their head office and manufacturing facility in San Diego, California.

RFMW
www.rfmw.com

Dataforth's modular data acquisition system at Acceed

The MAQ20 is the new data acquisition system from the US manufacturer Dataforth. The system distinguishes itself with its modular structure for space-saving and fast top-hat rail assembly as well as top cost efficiency per channel. All the system components and the software packages for analysis and graphic depiction of the measurement data are available from the German distributor Acceed. Designed for industrial data acquisition, measurement analysis and signal processing, the system consists of a communication module as a controller unit, the backplane for wiring and up to 24 individual I/O modules with an overall capacity of 384 channels.

Acceed GmbH
www.acceed.com

Distributor bundles 3D printer with modelling software

Distributor RS Components says it is making 3D printing more economical with a 40% price reduction on the FDM 3D printer, when purchased with DesignSpark Mechanical direct-modelling add-on software modules, to brings 3D design and fast prototyping capabilities to a wider audience of engineers. RS Components is offering a special bundle that combines advanced 3D modelling software and 3D printing hardware, and which provides advanced and highly affordable 3D design and prototyping capabilities. From the 1st December 2015, RS is offering a 40% reduction in price of the RS IdeaWerk 3D printer when purchased with the DesignSpark Exchange and DesignSpark Drawing add-on software modules.

RS Components
www.rs-online.com

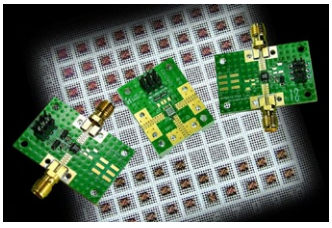
Over 900 RF power amplifiers added to MDL range

A new distribution agreement with Bonn Elektronik has enabled MDL Technologies to greatly expand its range of RF power amplifiers, with the addition of over 900 standard models. The instruments are available with frequencies ranging from 4 kHz up to 50 GHz, with power outputs from 1 W to 20 kW continuous wave (CW) or 30 kW pulsed. They can be air or liquid cooled, resulting in a significant size reduction for applications where space is limited. In addition to the power amplifier systems, MDL also offers a range of components from Bonn Hungary Electronics, including RF modules and subsystems, directional couplers, diplexers and filters, EMI pre-amplifiers, power combiners, cellular repeaters, circulators, isolators and up and down converters.

MDL Technologies
www.mdltechnologies.co.uk

More Custom MMIC from Aspen Electronics

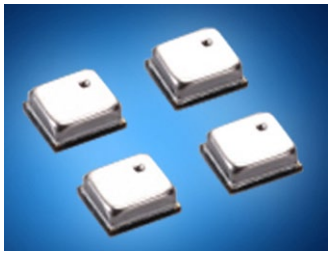
A bit of a misnomer but Custom MMIC, exclusively from Aspen Electronics, have steadily developed a range of catalogue monolithic microwave integrated circuits. 80% of the products the company now manufactures are standard, "off the shelf" designs. Custom MMIC boasts an extensive library of GaAs-based attenuators (digital and VVA), phase shifters (digital and analog), and switches (SPST, SPDT, and higher), that help circuit designers exercise precise control over the system in preparation. MMIC broadband low noise amplifiers are well suited for EW and communications systems where small size and low power consumption are needed.



Aspen Electronics
www.aspen-electronics.com

MEMS atmospheric pressure sensor offers 0.1% accuracy, in distribution

Mouser Electronics has the ZPA Series MEMS pressure sensor from Murata, a 2.3 × 2.6 mm micro-electro-mechanical systems (MEMS) sensor that provides highly accurate pressure readings from 300 to 1,100 hPa, down to 0.016 Pa resolution. The sensor employs capacitive sensing technology, which enables its ±1.0 hPa absolute accuracy across a wide temperature range (-10 to +65C; P=800 to 1,100 hPa). This capacitive sensing technology enables a low typical noise level of 1.1 PaRMS and current consumption of 6.3 µA at 0.16-second conversion time.



Mouser
www.mouser.com

The great IoT threat: how to avoid common security pitfalls during application development

By Calum Barnes

The future potential of the Internet of Things has been well documented. Cisco Systems estimates 25 billion devices will be connected to the internet by the end of this year, while IDC believes $7.3 trillion in revenue will be generated by IoT components by 2017. For entrepreneurs and big businesses alike, those figures are enticing enough to inspire the creation of a seemingly 'new' connected product, service or feature.

However the race to be first to market can result in quick and hasty decisions. Although the IoT is still young, there is already growing concern that poor application development and design are too often the rule rather the exception. With no real limitations to the kinds of historically "dumb" devices which can be made "smart," many IoT security failures can be traced back to poor decisions about the type of 'smart' features implemented, how they are implemented and the scope in which they will be used. However, IoT companies can learn something from the security advancements that have been made in the IT industry over the last 20+ years.

"Building an IoT product is not as simple as it might seem and quicker never means safer", says Calum Barnes, Xively Product Owner at LogMeIn.

The consumerisation of IT means that technologies designed and marketed to consumers often find their way into workplaces. It is nearly impossible to know how your technology will be applied once it has been marketed and sold. In an age where data breaches are making headlines on a daily basis, it's potentially disastrous for a business to not build in the proper security measures within product development. The IoT brings with it immense opportunity, but it could quickly be brought to its knees if manufacturers fail to consider security implications in their rush to hit the market place with 'the next big thing'. For business application developers, the following will help ensure security remains a priority throughout the development process:

#1 Secure your apps by design

Before beginning any app development, designers must weigh up the pros of 'connected' features against the cons of the security holes they open up. IoT applications must be designed to assess the security and privacy implications of connected features like messaging and social media integration upfront. An email proxy requires clear and concise directions on secure configuring, with strong administrator credentials, shielding it from low-level attacks and port scans. These basic protections will then influence other design decisions. A rigorous assessment of the security implications of smart features may increase the cost of development, but will save time and cost of flaws discovered down the road.

#2 Protect from inception to deployment

Connected device makers should also ensure any software updates or modification should require administrators to authenticate to the device first and require the use of signed executable files to verify the integrity of the software that is being installed. Devices must be able to register activity which could indicate an attack. Robust logging features are a must if administrators are required to recover compromised systems.

In today's IoT world, it's not enough to require end-users to use their initiative and set long passwords. There's a 'set and forget' mentality among users which is not sufficient for ensuring around-the-clock security.

#3 Avoid 'security through obscurity'

Another common mistake at the development phase is the dangerous 'security through obscurity' approach, i.e. the assumption that hackers won't be interested in your product. Products must be designed with the assumption that they will be purchased, dissected and studied. Security shortcuts such as embedded private keys or weak authentication might save time and speed up deployment, but a global IT ecosystem can quickly become a global botnet network.

#4 Don't make your supply chain the weakest link

You can't underestimate the importance of screening supply chain partners closely, to make sure contracts and service provider agreements protect you. By using emerging hardware security technologies, companies can remove the risk of malicious vendors or manufacturers. These technologies allow all secret keys or intellectual property to be secured and verified directly on the chip. This same approach can also protect you against device cloning or counterfeiting.

#5 Put Safety first

While great security is an absolute must have, companies must also prepare for the failure of their security. It's not enough to just have great external security, systems must be designed with compromise in mind. Traditional IT systems have just started doing this by encrypting information inside databases in the event that it is compromised. IoT devices should ensure that critical functions of the device cannot be affected or compromised by 'smart' features. For example, as cars become more connected, manufacturers should separate systems to ensure that a hacker doesn't get the "keys to the kingdom" so to speak. For example, separating air bag deployment systems

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from infotainment systems in a car.

Unfortunately, building an IoT product is not as simple as just connecting your product to the internet.

And while it is tempting to rush to try to be first to market, quicker does not mean safer. The security and privacy issues raised by connected products are often subtle and complex. Any business looking to design and deploy applications must wrap a robust security policy around every decision. For companies with limited resources, IoT platforms-as-a-service can address many of the security and data integrity issues that riddle poorly designed IoT products. Such tools let you streamline secure communications based on industry-standard encryption protocols and extend fine-grained user provisioning to IoT products. This will also improve time to market, whilst also avoiding a rude awakening in the future.

Quantum cryptography can be hacked

By Jean-Pierre Joosting

Researchers from Linköping University and Stockholm University have discovered that energy-time entanglement — the method that today forms the basis for many systems of quantum cryptography — is vulnerable to attack.

"With this security hole, it's possible to eavesdrop on traffic without being detected. We discovered this in our theoretical calculations, and our colleagues in Stockholm were subsequently able to demonstrate it experimentally," says Jan-Åke Larsson, professor at Linköping University's Division of Information Coding.

Quantum cryptography is considered a completely safe method for information transfer, and theoretically it should be impossible to crack. Many research groups around the world are working to make quantum cryptography resistant to various types of disturbance, and so far it has been possible to handle the disturbance that has been detected. Quantum cryptography technology is commercially available, but there is much doubt as to whether it is actually used.

"It's mostly rumours, I haven't seen any system in use. But I know that some universities have test networks for secure data transfer," says Prof Larsson.

The energy-time entanglement technology for quantum encryption studied here is based on testing the connection at the same time as the encryption key is created. Two photons are sent out at exactly the same time in different directions. At both ends of the connection is an interferometer where a small phase shift is added. This provides the interference that is used to compare similarities in the data from the two stations. If the photon stream is being eavesdropped there will be noise, and this can be revealed using a theorem from quantum mechanics — Bell's inequality.

On the other hand if the connection is secure and free from noise, you can use the remaining data, or photons, as an encryption key to protect your message.

What the LiU researchers Jan-Åke Larsson and his doctoral student Jonathan Jogenfors have revealed about energy-time entanglement is that if the photon source is replaced with a traditional light source, an eavesdropper can identify the key, the code string. Consequently they can also read the message without detection. The security test, which is based on Bell's inequality, does not react — even though an attack is underway.

Physicists at Stockholm University have subsequently been able to demonstrate in practical experiments that it is perfectly possible to replace the light source and thus also eavesdrop on the message.

But this problem can also be solved.

"In the article we propose a number of countermeasures, from simple technical solutions to rebuilding the entire machine," explains Jonathan Jogenfors.

The article has been published in Science Advances.

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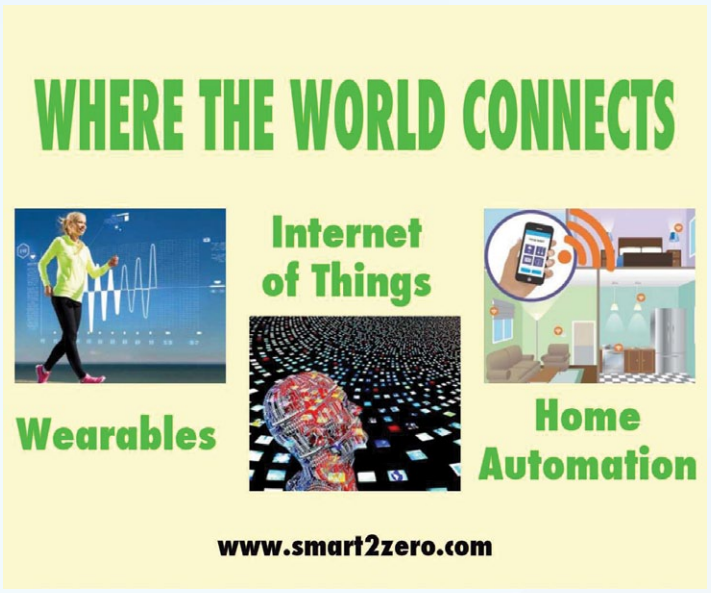

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